Lab. Manual

OPERATION & MAINTENANCE

HANDBOOK

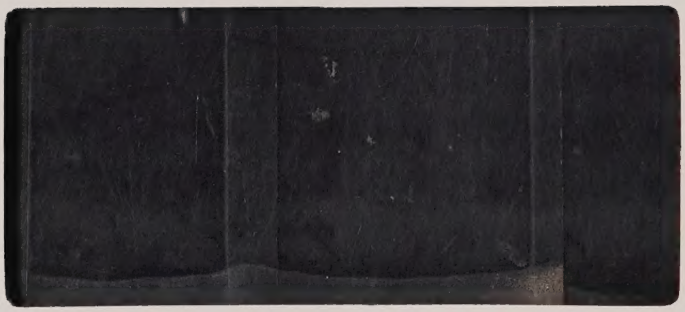
MODEL 213A
RANDOM DATA GENERATOR

PART NO. 37000-640

S/N 01059

DATAPULSE®

A SUBSIDIARY OF SYSTRON-DONNER CORPORATION



OPERATION & MAINTENANCE

HANDBOOK

MODEL 213A
RANDOM DATA GENERATOR

PART NO. 37000-640

S/N 01059

DATAPULSE
DIVISION
SYSTRON DONNER
CORPORATION

10150 W. JEFFERSON BLVD., CULVER CITY, CALIFORNIA 90230

THIRD EDITION

Printed in May, 1968
Reprinted in November, 1968
Reprinted, incorporating E.O's
and deleting Section IV February, 1969

Model 213A Random Data Generator

The Datapulse Model 213A Pseudo-random Data Generator and Error Detector is a truly unique instrument in its field. It is capable of generating pseudo-random data patterns at bit rates to 10 MHz. It can compare these patterns to external data patterns for the purpose of detecting errors in the external data. Also, worst-case patterns for a particular data system can be discovered by the cascading of two or more units for the production of extremely long random words. It is an indispensable tool for the data system designer and production test engineer.

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_06959

TABLE OF CONTENTS

			PAGE
SECTION I	SPECIFICATIONS AND OPERATION		
	1.1	Modes of Operation	1-1
	1.2	Operating Controls and Indicators	1-2
	1.3	Input Signal Specifications	1-4
	1.4	Output Signal Specifications	1-4
	1.5	Error Rate Contribution	1-5
	1.6	Additional Specifications	1-5
SECTION II	THEORY OF OPERATION		
	2.1	Shift Register	2-2
	2.2	Feedback Selection	2-2
	2.3	Feedback Generation	2-2
	2.4	Feedback Control	2-3
	2.5	Sync Selection	2-3
	2.6	Sync Generation	2-3
	2.7	Error Detection	2-3
	2.8	Error Hold	2-4
	2.9	Error Pattern Readout	2-4
	2.10	Single Pass Mode	2-4
SECTION III	MAINTENANCE AND CALIBRATION		
	3.1	Preventive Maintenance	3-1
	3.2	Troubleshooting	3-2
	3.3	Calibration	3-2

LIST OF SCHEMATICS:

Drawing Number	Title
41000-186	Block Diagram - Model 213A
41000-194	Logic Diagram - Feedback Generation
40000-224	Schematic Diagram - Schmitt Trigger
40000-228	Schematic Diagram - Oscillator-Clock
40000-315	Schematic Diagram - Output Buffer
40000-316	Schematic Diagram - Single Pass Mode
40000-317	Schematic Diagram - Clock Control
40000-318	Schematic Diagram - Sync Length Cont.
40000-323	Schematic Diagram - Mode Control
40000-324	Schematic Diagram - Error Pattern Readout
40000-325	Schematic Diagram - Sync Pattern Generation
40000-326	Schematic Diagram - Sync Pattern Select
40000-327	Schematic Diagram - Error Hold and Feedback Control

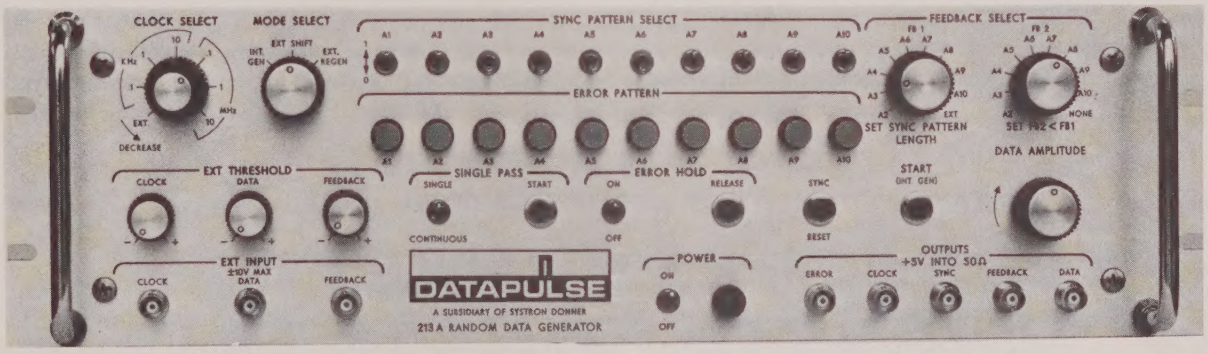
LIST OF SCHEMATICS:

Drawing Number	Title
40000-329	Schematic Diagram - Feedback Selection
40000-330	Schematic Diagram - Shift Register
40000-331	Schematic Diagram - Input/Output Controls
40000-332	Schematic Diagram - Register Loading
40000-352	Schematic Diagram - Power Supply

SECTION I

SPECIFICATIONS AND OPERATION

This combined description of the instrument's specifications and operating controls will provide the user with a thorough understanding of the operation and capabilities of the Model 213A. Reference to the front panel photograph, shown below, or to an actual instrument will greatly enhance your study of the following descriptions. All referenced drawings will be found at the back of this manual.



Front Panel, Model 213A

1.1 MODES OF OPERATION

The Model 213A performs several data generating and testing functions through the selection of one of its three major modes of operation by the MODE SELECT switch, S2 (Drawing number 40000-323).

1.1.1 Internal Generate Mode

In this mode, the 213A generates pseudo-random data sequences. The start of the sequence is established by the sync pattern select switches and the data content of the output is determined by the feedback select switches. Generation of fixed data words (2 to 10 bits long) may be accomplished in this mode through proper feedback selection.

1.1.2 External Regenerate Mode

The 213A is used to test the capability of other data handling equipment by operating it in this mode. The data output from the external equipment is fed into the 213A. Upon receipt of a data pattern corresponding to the selected sync pattern, it generates a pseudo-random data sequence, beginning with the next sequential bit, in the manner described above. It compares this internally generated data, bit for bit, with the externally supplied data and provides signals corresponding to the errors detected. Clock synchronization between the external and internal data is required in this mode.

1.1.3 External Shift Mode

Operation begins in this mode, as in the external regenerate mode described above, with receipt of a data pattern from an external source which corresponds to the selected sync pattern. It then proceeds to continuously use the content of the previously received external data to generate the next bit in the sequence and, as before, provides error detection. The principle function of this mode is to allow pattern expansion, through the cascading of two or more generators, to yield statistically improved test results.

1.2 OPERATING CONTROLS AND INDICATORS

1.2.1 Clock Select

The CLOCK SELECT switch, S1 (Drawing number 40000-317), selects the basic system clock rate range. Vernier potentiometer, R1 (Drawing number 40000-317), provides continuous control through each range. Clock rates from 10 Hz to 10 MHz may be set by internal oscillator (Drawing number 40000-228) or by an externally supplied signal as specified below.

1.2.2 Mode Select

The MODE SELECT switch, S2 (Drawing number 40000-323), selects any of the operational modes described above.

1.2.3 Sync Pattern Select

The starting pattern of the pseudo-random sequence, in all operating modes, is selected by the SYNC PATTERN SELECT switches, S5 through S14 (Drawing number 40000-326).

1.2.4 Feedback Select

FEEDBACK SELECT switches FB1 and FB2, S3 and S4, respectively, (Drawing number 40000-329) select the shift register stages to be used in the modulo two adder feedback circuit. The externally supplied feedback signal described below may also be selected.

1.2.5 External Threshold

Three EXTERNAL THRESHOLD controls, CLOCK, R2; DATA, R3; and FEEDBACK, R4; (Drawing number 40000-331) are provided which set the triggering level for the externally supplied signals specified below.

1.2.6 Single Pass

SINGLE PASS toggle switch, S15 (Drawing number 40000-323), allows continuous repetitive cycling of the selected data sequence or a single cycle of the sequence as initiated by the SINGLE PASS START pushbutton switch, S16 (Drawing number 40000-323).

1.2.7 Error Pattern

Ten ERROR PATTERN indicator lamps, DS1 through DS10 (Drawing number 40000-324), light to indicate a difference in data content between an externally supplied data signal and the corresponding shift register stage.

1.2.8 Error Hold

The ERROR HOLD toggle switch, S17 (Drawing number 40000-323), allows continuous operation regardless of error or stops the system and holds the error indication as each error is detected. The RELEASE pushbutton switch, S18 (Drawing number 40000-323), restarts operation after each hold.

1.2.9 Sync Reset

The SYNC RESET pushbutton switch, S19 (Drawing number 40000-323), resets the sync circuits to await receipt of the selected sync pattern.

1.2.10 Start (Int. Gen.)

The START (INT. GEN.) pushbutton switch, S20 (Drawing 40000-323), starts the generation of a data sequence in the internal generate mode.

1.2.11 Data Amplitude

Potentiometer R5 (Drawing number 40000-331), varies the DATA OUTPUT amplitude as specified below.

1.3 INPUT SIGNAL SPECIFICATIONS

Externally supplied CLOCK, DATA, and FEEDBACK signals which exhibit the following characteristics may be supplied to the 213A through their respective connectors: J40, J41, and J42 (Drawing number 40000-331). Note that a threshold control (described above) is provided to set the level at which each input triggers the system.

1.3.1 Maximum Clock Rate

10 MHz.

1.3.2 Minimum Duration (Clock Input only)

30 ns

1.3.3 Input Amplitude

The 213A will trigger on a ±1 to ±5 volt signal.

1.3.4 Input Impedance

Approximately 1 K

1.4 OUTPUT SIGNAL SPECIFICATIONS

The five system output waveforms, ERROR, CLOCK, SYNC, FEEDBACK, and DATA, exhibit the following characteristics when their respective output connectors, J43, J44, J45, J46, and J47, (Drawing number 40000-331) are properly terminated with a 50Ω resistive load.

1.4.1 Amplitude (with respect to ground)

The DATA output is continuously variable from +0.6 volts to +5 volts. All other outputs exhibit a fixed amplitude of +5 volts ±10%.

1.4.2 Transition Time

Less than or equal to 10 ns

1.4.3 Format (Data and Feedback)

NRZ

1.5 ERROR RATE CONTRIBUTION

Self-generated errors in the 213A are no greater than one part in 10^8.

1.6 ADDITIONAL SPECIFICATIONS

1.6.1 Power Required

105/125 volts, 50/60 Hz ac, approximately 5 W

1.6.2 Physical Dimensions

5-1/4" high by 19" wide by 20" deep

1.6.3 Weight

Approximately 30 lbs

1.6.4 Operating Temperature

The 213A is rated for operation with ambient temperature from 0 to 50°C.

1.6.5 Signal Connectors

Type BNC

1.6.6 Accessories Furnished

One 8-foot line cord with 3-prong power plug, one operation and maintenance handbook, and one IC card extender.

SECTION II

THEORY OF OPERATION

Pseudo-random data is finding increased usage in the testing of various types of data storage and transmission systems. This includes long duration storage such as tape and core storage as well as short duration storage such as delay lines. At times these systems exhibit sensitivities to particular patterns of data. The testing problem becomes first, that of determining if such a worst-case pattern exists, and second, that of discovering what the pattern is. Depending upon the type of system being tested, it may or may not be possible to determine the existence and/or characteristics of a worst-case pattern prior to the actual testing. In the case where the pattern characteristics are known, the problem reduces itself to that of simply setting that pattern into a conventional data generator. If the pattern is not known, the first step is to determine whether such a pattern exists. One method would be to use a normal data generator and manually try all possible patterns. This technique is extremely time consuming and expensive. Another method is to use a random data generator that would generate all possible patterns. The problem with this approach is that the detection and identification of the pattern within a random sequence becomes extremely difficult, and the sequence cannot be repeated for further testing. What is needed then is a form of data which has the statistical characteristics of random data but that can be exactly repeated when needed. This is pseudo-random data. Detection and identification of problem patterns with this form of data can be accomplished quite simply.

In the 213A the pseudo-random data is generated by means of a 10-stage shift register. Feedback is provided for the shift register input by a modulo two adder. The feedback consists of the exclusive OR'ed combination of two selected shift register stages. By proper setting of the feedback select controls, various length pseudo-random sequences can be generated. The maximum length sequence that can be generated by a shift-counter of this type is 2^n-1 bits in length when n is the number of stages in the register. Since the 213A employs a 10-stage register, the maximum length sequence that it will generate contains 1023 bits. If only one stage of the register is used for feedback, short fixed patterns of 2 to 10 bits can be generated.

To provide for synchronization with external data, the 213A employs a sync circuit which monitors each stage of the shift register. When the register contains the preselected number, a sync pulse is generated. Since the sync number is selectable, any desired point in the sequence may be used as reference. The sync pulse is made available as an output as well as being used internally to synchronize the 213A with incoming data.

In order to determine whether or not a problem pattern exists, we must have some way of comparing the incoming data to be tested with what it should be. The 213A accomplishes this by feeding the incoming data and the internally generated feedback into an exclusive "OR" type comparator. This allows a bit for bit comparison and any time the two signals are not logically

equal, an error signal is generated. The error pulse may be externally counted to determine system error rate or, by use of internal circuitry, used to interrupt the 213A at error time. When this mode of operation is used, the preceding ten bits of the generated sequence are displayed on the front panel of the 213A. The least significant digit of the displayed number shows the proper state of the particular bit that was in error.

In some types of testing, it may be desirable to generate a burst of pseudo-random data rather than a continuous stream. The 213A offers this capability by the addition of a SINGLE PASS mode. In this mode a single sequence is generated for each operation of a front panel pushbutton. The length of the sequence is determined by the FEEDBACK SELECT controls as when running continuously. This single word or sequence may be synchronized with external data in which case the word starts upon receipt of the selected sync pattern. The 213A then generates the desired word and stops. This process may be repeated by resetting the sync circuit.

2.1 SHIFT REGISTER (Drawing number 40000-330)

The shift register is a 10-stage circuit using high speed TTL J-K flip-flops. The first 8 stages are located at J10; stages 9 and 10 are located at J12. The true and complement logic signals from all stages are brought out at the register. Both dc set and reset lines are also provided for each stage. Clock drive for the register has been split for loading purposes. Stages 1, 2, 3, 4, and 9 are driven by CP-A from J14-(11), while stages 5, 6, 7, 8, and 10 are driven by CP-B from J14-(12).

2.2 FEEDBACK SELECTION (Drawing number 40000-329)

Feedback selection is controlled by 2 ten-position rotary switches located on the front panel. Each switch provides a logical "1" (+5V) for the selected position and a logical "0" (GRD) for all other positions.

2.3 FEEDBACK GENERATION (Drawing number 40000-328)

Feedback generation logic is composed of programmer card J22 and the exclusive "OR" circuit consisting of gates (1), (2), (3), and (4) on J24. Each feedback selection switch controls one-half of the programmer card. As a given stage is selected, the true output from that stage is gated through the card and into one side of the exclusive "OR" circuit. The output of this circuit (internal feedback) is sent to the feedback control logic at J18-(4) and J26-(2) and to the error detection logic at J18-(6), (7). Test points are provided for each half of the feedback programmer, and the combined feedback signal can be monitored at J24-(4).

2.4 FEEDBACK CONTROL (Drawing number 40000-327)

Feedback control is accomplished by gates (4), (5) on J18 and gates (1), (2), and (3) on J26. When operating in the internal generate mode, the internally generated feedback is gated through to the input of the shift register. In the external regenerate mode the external data is gated through to be used as feedback until the selected sync pattern is received. Upon receipt of the selected sync pattern, the external data is gated off and the internally generated feedback is used to drive the register. In the third mode of operation, external shift, the external data only is used as feedback to the register. The output of the feedback control is sent directly to stage A1 of the shift register and also to gate (12) on J18 to provide the complement signal for A1. The "true" feedback is provided as an output on the front panel.

2.5 SYNC SELECTION (Drawing number 40000-326)

The desired sync pattern is selected by 10 toggle switches located on the front panel. Each switch corresponds to a stage in the shift register. The outputs of the switches are sent to the sync generation card at J20. The sync select switches are also used to preset any desired number into the shift register. For this operation a portion of each switch is used to control the dc set and reset inputs to each register stage. Preset is initiated by operation of the START (INT GEN) pushbutton on the front panel.

2.6 SYNC GENERATION (Drawing number 40000-325)

The generation of sync pulses is accomplished by a 20-section programmer located at J20. The true and complement outputs of each shift register stage and 20 corresponding outputs of the sync select switches are used as inputs to the programmer. The outputs of the sync programmer are two sync signals, each one corresponding to one-half of the shift register. These outputs are combined by gates (1), (2), (3) on J18. Gate (6) on J34 is used to invert the sync pulse for use by the sync output buffer and the single pass mode logic. Flip-flop (6) on J12 is set by the sync pulse to be used in the feedback control logic as discussed above. The sync flip-flop is reset by operation of the SYNC RESET pushbutton on the front panel.

2.7 ERROR DETECTION (Drawing number 40000-327)

Data errors are detected by the use of gates (6), (7), (8), and (9) on J18 and gate (4) on J26. The use of gate (4) on J26 insures that error signals are generated only after the 213A has achieved synchronization with the incoming

data. This is accomplished by "ANDING" the dc sync signal and the clock with the actual detected error as provided by gate (9) on J18. The error pulse is then fed through inverter (7) on J34 to the error output buffer. The noninverted error pulse is sent to J34-(9) for use in the ERROR HOLD mode as discussed below.

2.8 ERROR HOLD (Drawing number 40000-327)

The ERROR HOLD mode is used to stop the 213A at any time an error signal is generated. Flip-flop (5) on J12, as well as gates (9), (10), and (11) on J34, and gate (10) on J18, are used to interrupt the shift register clock pulses upon receipt of an error signal from the error detector circuitry. Gates (9) and (10) on J34 act as a toggle flip-flop. The negative true error signal sets gate 9 to a logical "1". This signal is sent to (11) on J34 to gate through the next CP to the set input of flip-flop (5) on J12. The "true" output of F/F (5) is AND'ed with the ERROR HOLD select switch at (10) on J18. If the ERROR HOLD mode is selected, a logical "0" is sent to one input of gate (5) on J26 through which all register clock pulses are gated. The clock pulses are thus interrupted until this logical "0" is removed by resetting the ERROR HOLD F/F (5) by operation of the ERROR HOLD RELEASE pushbutton on the front panel. The ERROR HOLD "0" is also sent to inverter (11) on J18 to form the read error signal. The use of this signal will be discussed below.

2.9 ERROR PATTERN READOUT (Drawing number 40000-324)

The read error signal generated above is sent to the lamp driver card at J14 and applied to one side of each of 10 power NAND gates. The other inputs to these gates are the "true" outputs of the shift register. The gate outputs are connected to one side of each error indicator lamp on the front panel. When the read error signal is received the indicator lamps corresponding to register states in the "1" condition will be illuminated. The operation will take place only when in the ERROR HOLD mode.

2.10 SINGLE PASS MODE (Drawing number 40000-316)

The SINGLE PASS mode allows for the generation of a single pass through the selected pseudo-random sequence. It may be used in either the internal generate or the external regenerate mode. The logic for this function

is contained on J16 gates (1) through (12) and J12-F/F (3) and (4). Its use in the internal generate mode will be discussed first. During continuous operation ($\overline{\text{Single Pass}}$) clock pulses are gated through gates (11) and (12). For this to occur, one of the inputs to NOR gate (10) must be at a ground (logical "0") level This can be either from the single pass/continuous switch being in the CONTINUOUS position or from F/F (4) being in the set condition.

Initial conditions for the single pass mode are the SINGLE/CONTINUOUS switch in the SINGLE position, F/F (3) reset, and F/F (4) reset. Operation of the SINGLE PASS START pushbutton applies, through gates (2), (3), and (4), a dc set signal to F/F (3) and applies a logical "0" to the 'J' input to F/F (4). As the pushbutton is released the 'J' input to F/F (4) returns to a "1". The set condition of F/F (3) allows clock pulses to be gated through gates (8) and (9) to F/F (4) which allows it to set. The set condition of F/F (4) now allows clock pulses to be gated through gates (11) and (12) to the shift register. Since the START pushbutton also presets the shift register to the number contained in the sync select switches, the generated sequence starts with the first bit following the selected sync pattern. As the sequence passes through the sync pattern again, the generated sync pulse is "ANDed" with the CP at (5), inverted by (6), (7) and used to reset F/F (4). As F/F (4) is reset the clock pulses are inhibited and the sequence is stopped. The 213A has thus generated a complete sequence from one sync pattern to the next.

When operated in the external regenerate mode the operation is similar with the exception that the 213A does not achieve synchronization until the selected sync pattern is received in the external data. It continues to generate the sequence until the next sync pattern is received at which time it stops. Since error checking is only done while the 213A is in sync, this provides one complete sequence of error checking.

SECTION III

MAINTENANCE AND CALIBRATION

The Model 213A has been designed to keep the requirement for maintenance and calibration at a minimum. This section of the manual sets forth a number of suggestions for the maintenance, calibration, and troubleshooting of the instrument which, in conjunction with the circuit theory discussion, block diagram and schematic diagrams, should enable the user to maintain it with a minimum of difficulty.

3.1 PREVENTIVE MAINTENANCE

A regularly scheduled routine of preventive maintenance is recommended to attain the full potential usable life of the equipment. The following suggestions should be followed, as a minimum.

3.1.1 Visual Inspection

Perform a complete visual inspection at regular intervals, preferably once a month. Inspect for loose or broken connections; damaged binding posts; scorched printed circuit boards, wires or resistors; and loose nuts and bolts.

For most visual troubles, the remedy is apparent; however, particular care must be taken when heat-damaged components are detected. Overheating of parts is often the result of other, less apparent defects in the circuit.

3.1.2 Component Replacement and Soldering Considerations

When replacing transistors, diodes, or other heat-sensitive devices, a heat sink should be used between the device and the soldering iron tip. A pair of long-nosed pliers may be used in most cases.

Special care must be taken when soldering printed circuit wiring to avoid overheating and subsequent separation of the printed circuit from its epoxy material.

3.1.3 Power Cable

The three-conductor power cable supplied with this instrument is terminated in a polarized three-prong male connector as recommended by the National Electrical Manufacturer's Association. The third contact is an offset round pin which is added to a standard two-blade connector and grounds the instrument chassis when used with an appropriate receptacle.

3.2 TROUBLESHOOTING

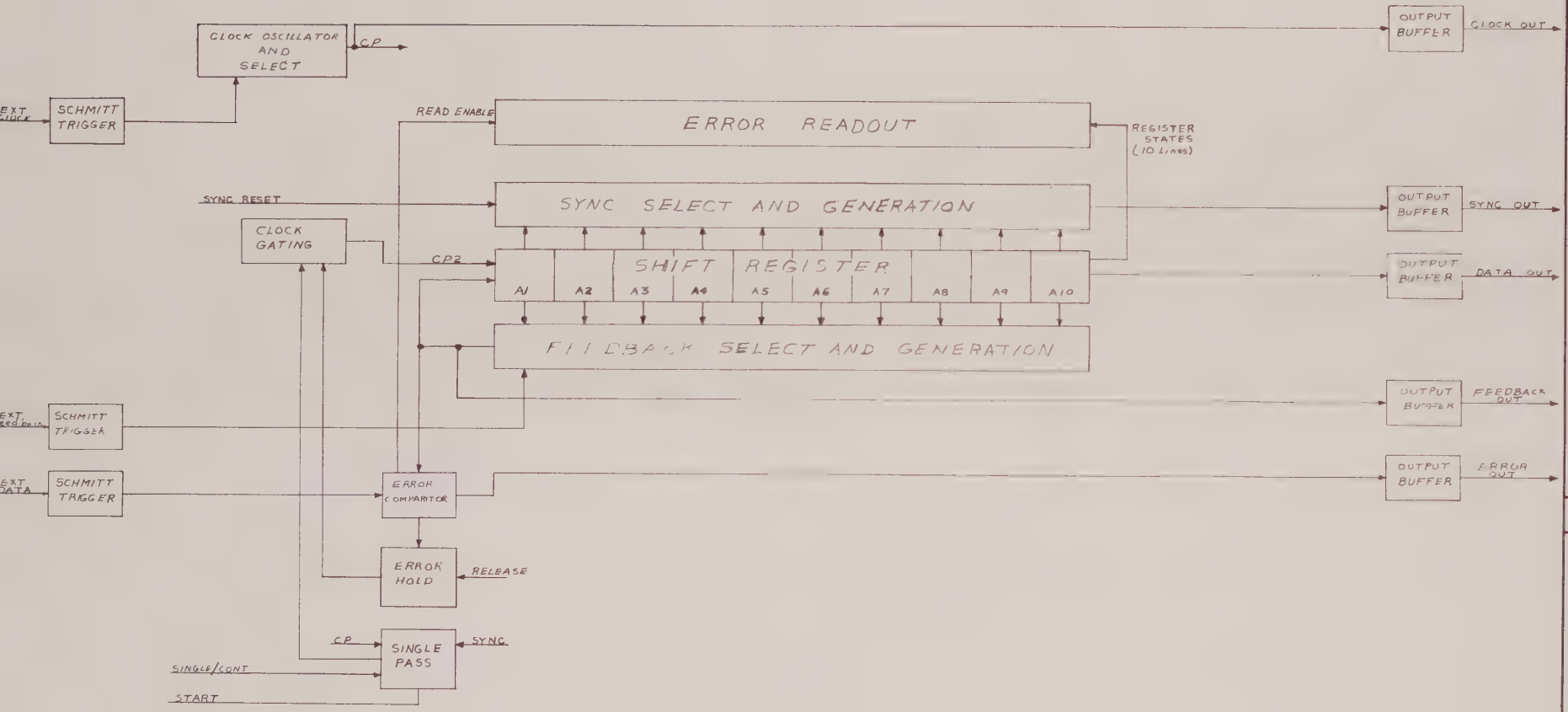
The easiest and most convenient method of troubleshooting the Model 213A is replacement of faulty functions at the card level. This method reduces troubleshooting to a check of power supply voltages, a determination of the faulty card, and replacement of same. Inoperative cards should then be returned to the factory where they will be quickly repaired or replaced. It is recommended that a set of spare cards be purchased for purposes of troubleshooting. Replacements can be arranged at any time, however, through Datapulse or your local Datapulse representative.

3.3 CALIBRATION

3.3.1 Clock Rate

The clock is first adjusted on the 10 MHz range with the vernier set to max (CW). Adjust R (2K) for a max clock rate of 10 MHz. The vernier is then set to the minimum position (CCW). Adjust R (100K) for a clock rate of 1 MHz. Recheck 10 MHz adjustment. The lower ranges should then be checked to insure overlap between ranges.

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES			
TOLERANCES ON			
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	
MATERIAL			
FINISH			
DO NOT SCALE DWG			

DRAWN		
CHECKED		
APPROVED		
APPROVED		
APPROVED		
RELEASED		

TITLE

BLOCK DIAGRAM

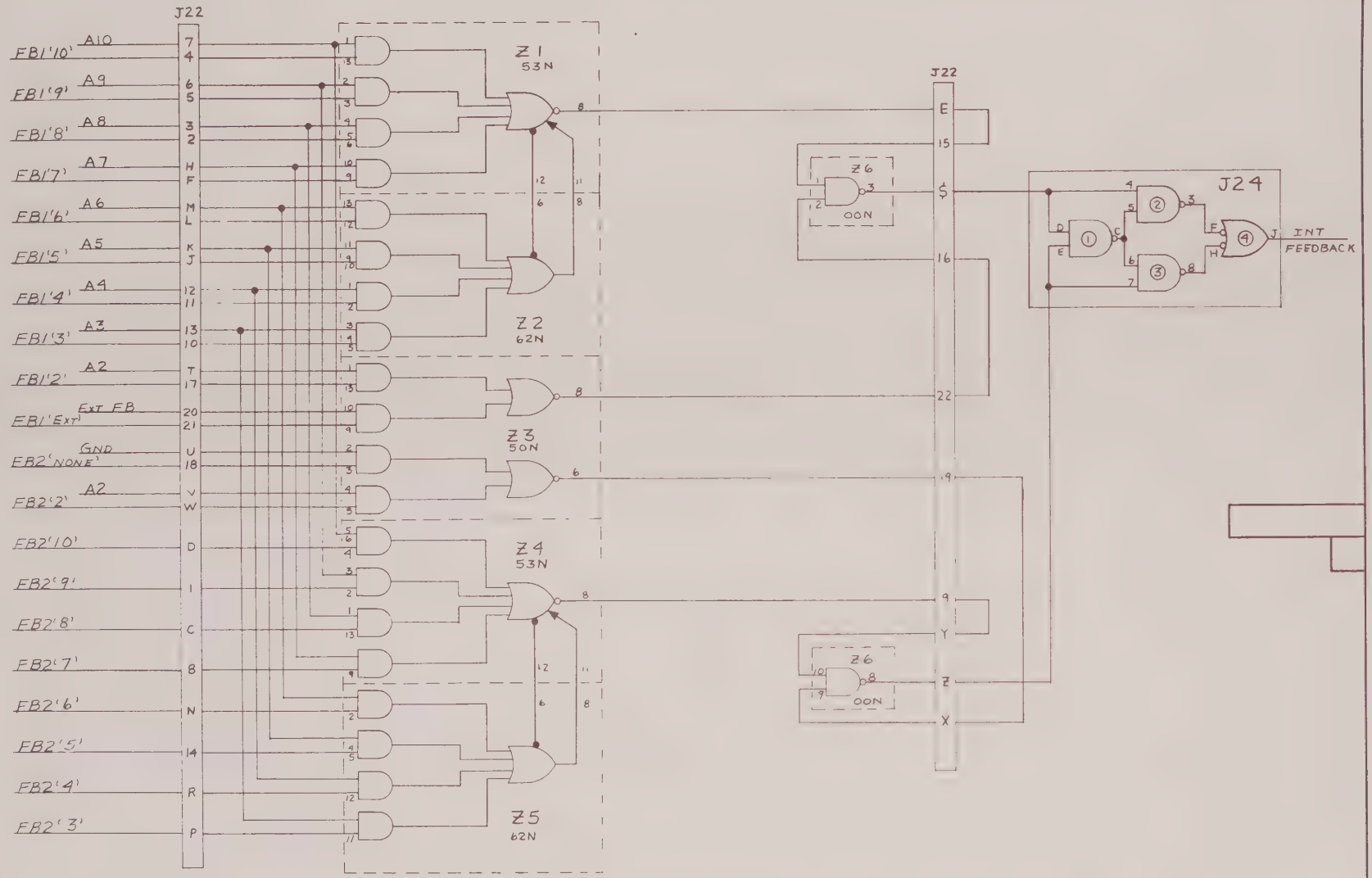
MODEL 213A

DATAPULSE

DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG	
SIZE C	41000 - 186

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES			
TOLERANCES ON			
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	
MATERIAL			
FINISH			

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DO NOT SCALE DWG.

DRAWN		1/8/68
CHECKED		1/8/68
APPROVED		1/8/68
APPROVED		
APPROVED		
RELEASED		

TITLE

LOGIC DIAGRAM FEEDBACK GENERATION Model 213A

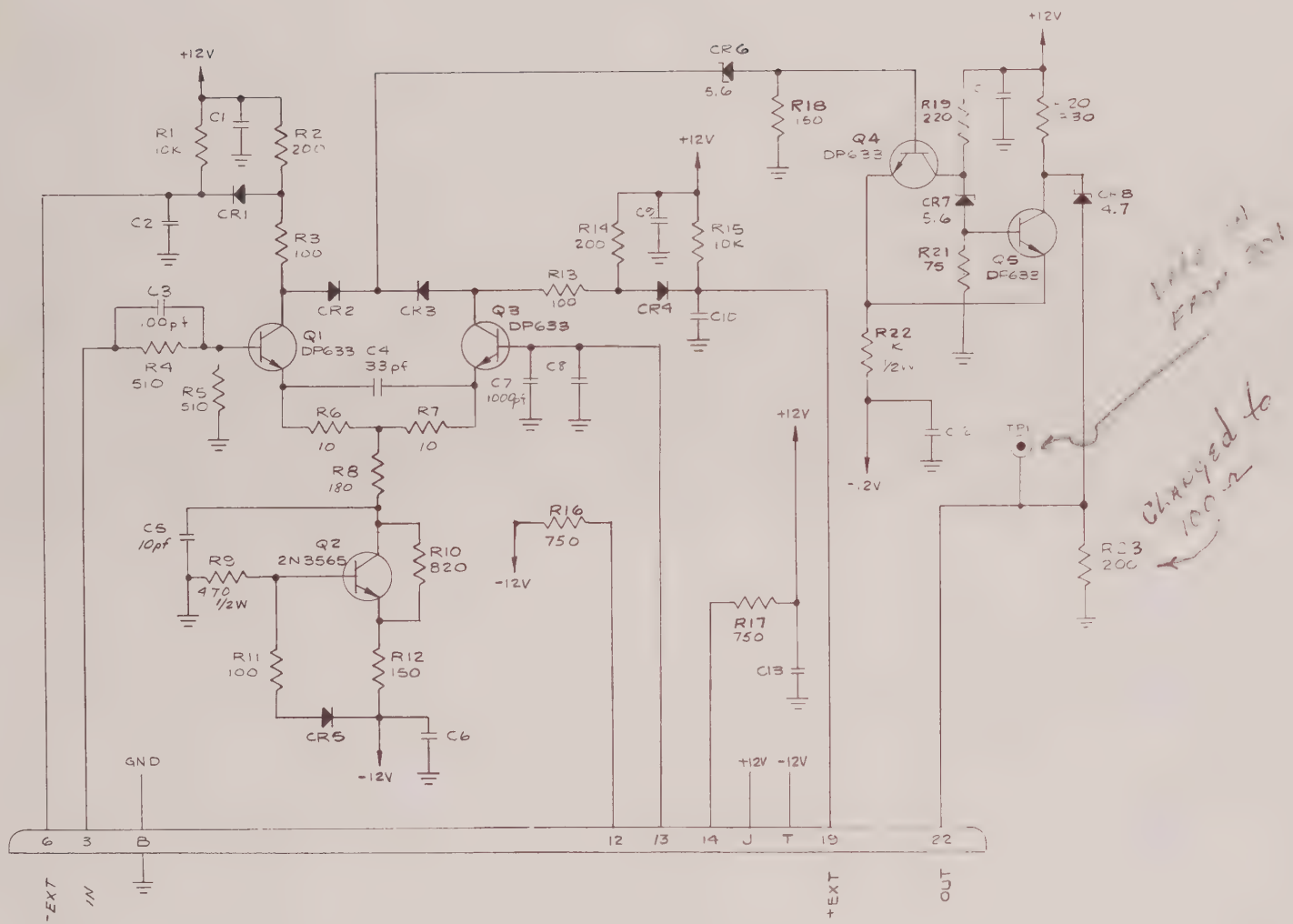
DATAPULSE

DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG	
SIZE C	41000-194
SCALE	CODE 15933
SHEET 1	OF 1

K-E ALBANENE® LA 2722

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



Changed to 100Ω

3 ALL CAPACATORS ARE .022 μf

2 ALL RESISTORS ARE IN OHMS, 5% 1/4W

1 ALL DIODES ARE DP16-0

NOTES - UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
3 PLACE DEC. ± | 2 PLACE DEC. ± | ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DWG.

DRAWN N.Chapman 2/28/68
CHECKED
APPROVED
APPROVED

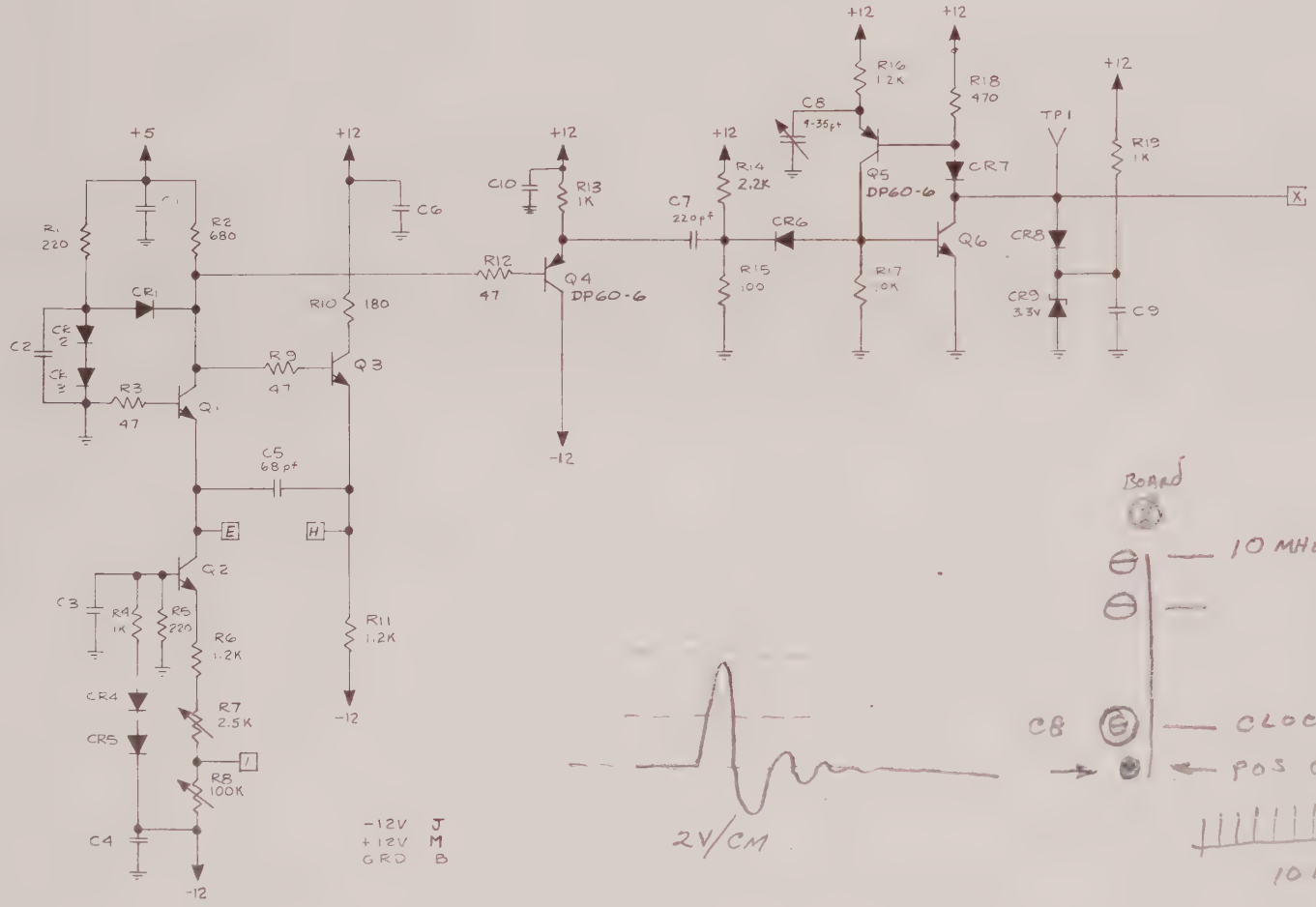
TITLE
SCHEMATIC DIAGRAM
SCHMITT TRIGGER
MODEL 213A

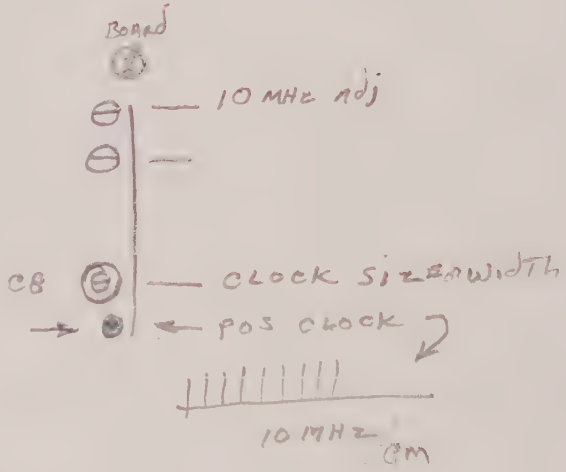
SCALE NONE

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG C SIZE 40000-224
SHEET 1 OF 1

REVISIONS				
ECN	SYM	DESCRIPTION	DATE	APPROVAL





3. ALL CAPACITORS ARE .022μf
2. ALL TRANSISTORS ARE TYPE DP63-3
1. ALL DIODES ARE TYPE DP16-0
NOTES: UNLESS OTHERWISE SPECIFIED

J2

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

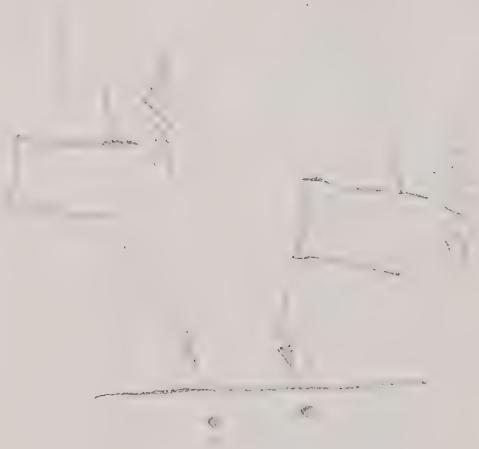
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
3 PLACE DEC. ± | 2 PLACE DEC. ± | ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DWG.

DRAWN		
CHECKED		5/2/11
APPROVED		5/3/11
APPROVED		
APPROVED		
RELEASED		

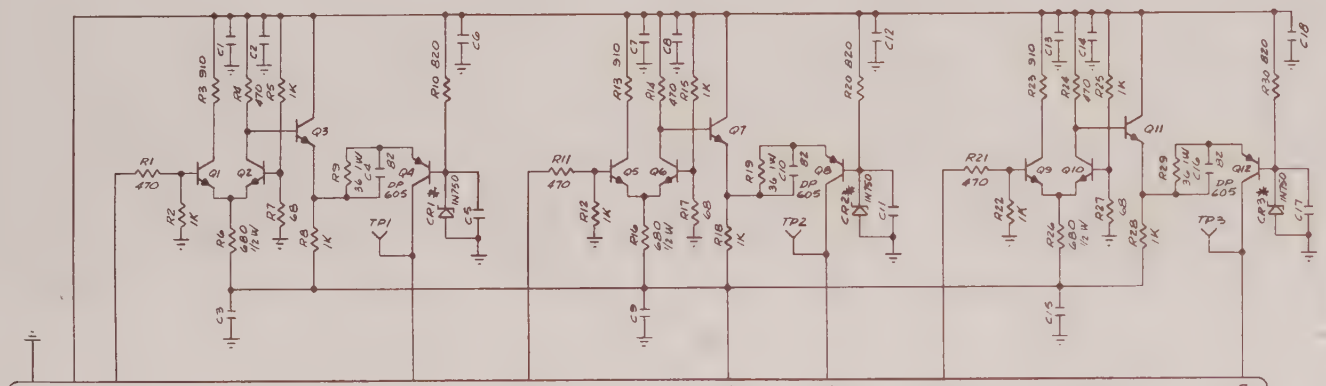
TITLE
SCHEMATIC DIAGRAM
OSCILLATOR - CLOCK
MODEL 213A
SCALE

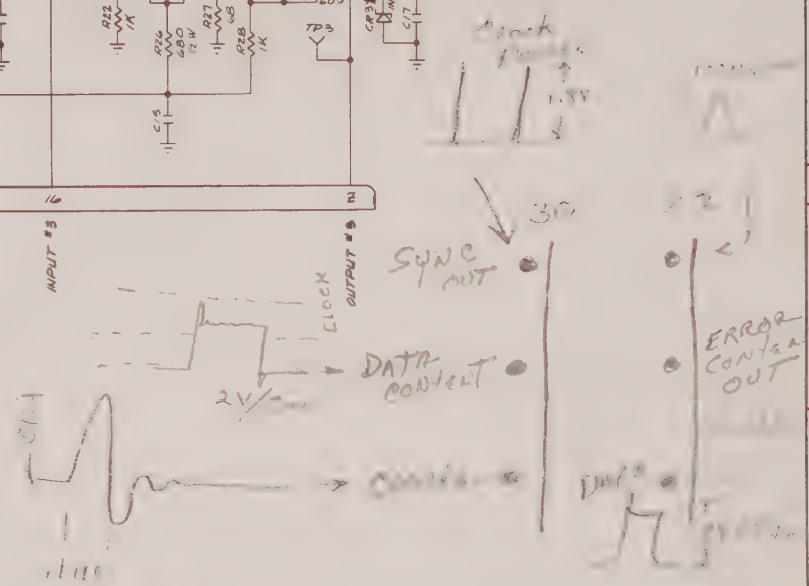
DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG C SIZE 40000 - 228
SHEET 1 OF 1



REVISIONS				
ECN	SYM	DESCRIPTION	DATE	APPROVAL
2635	A	1) ADDED NOTE 4 2) ADDED * TO CR1, 2, 3		





4. * INDICATES FACTORY ADJUST (MAY OR MAY NOT BE PRESENT)
3. ALL TRANSISTORS ARE DP63-3
2. ALL CAPACITORS ARE .022 μf
1. ALL RESISTORS ARE 1/4 W, ±5%

NOTE: UNLESS OTHERWISE SPECIFIED

J30
J32

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DO NOT SCALE DWG.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
3 PLACE DEC ± | 2 PLACE DEC. ± | ANGLES ±
MATERIAL
FINISH

DRAWN	Awd	6/3/68
CHECKED		6/6/68
APPROVED		6/6/68
APPROVED		
APPROVED		
RELEASED		

TITLE
SCHEMATIC DIAGRAM
OUTPUT BUFFER
MODEL 213A

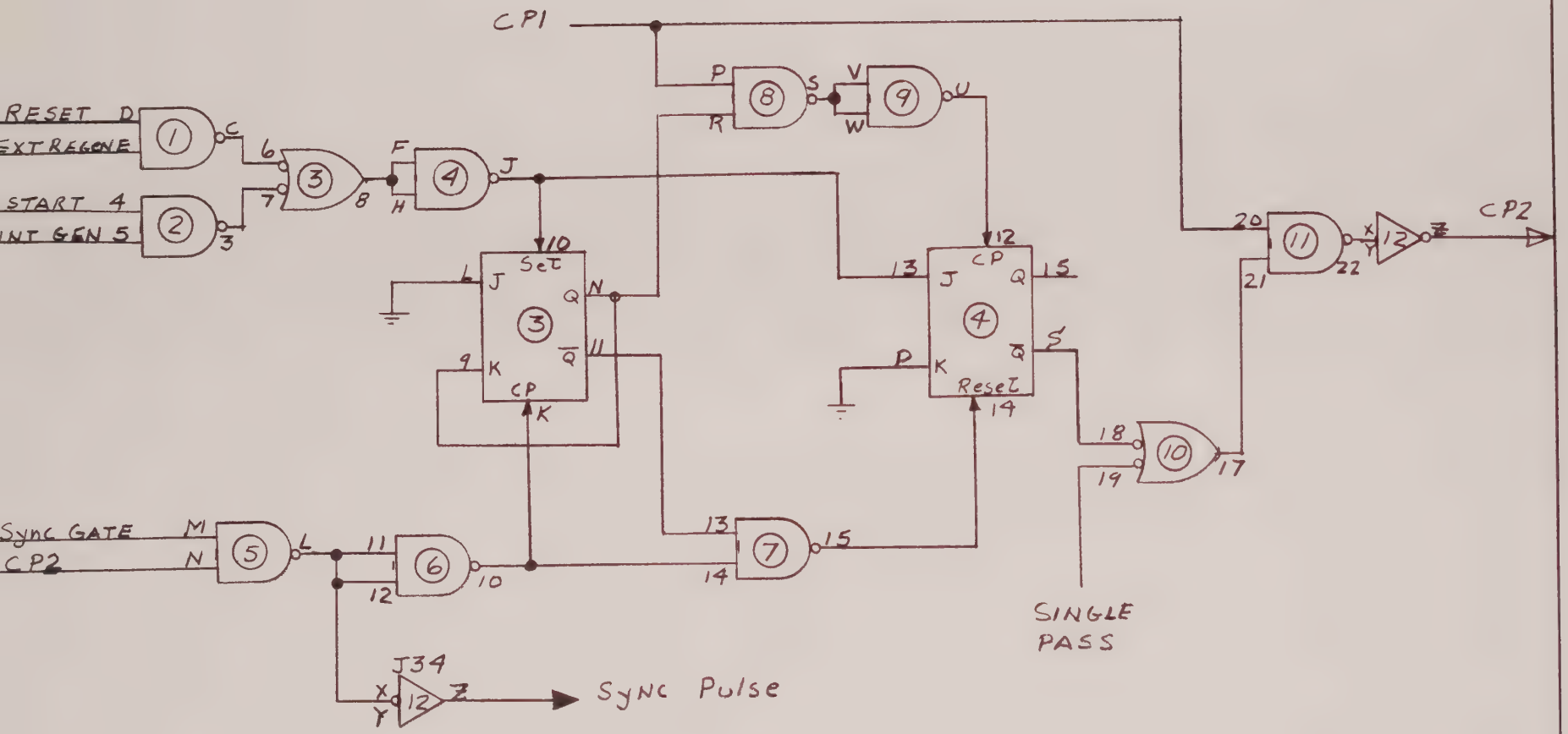
SCALE

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG C SIZE 40000-315

SHEET 1 OF 1

40000-315 | A |



2 Nand on J16

F/F on J12

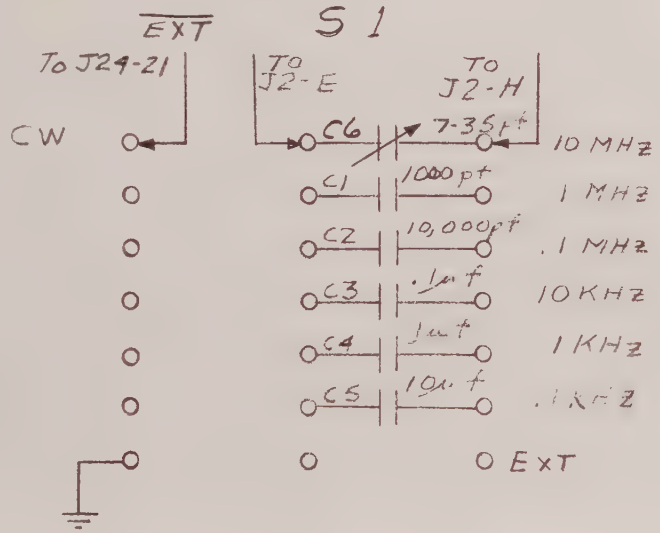
REVISIONS	APPROVALS		DATE	TITLE
DWN			8/9/69	SCHEMATIC DIAG
CKD			8/9/69	SINGLE PASS MODE
APPD			8/9/69	MODEL 213A
REL				

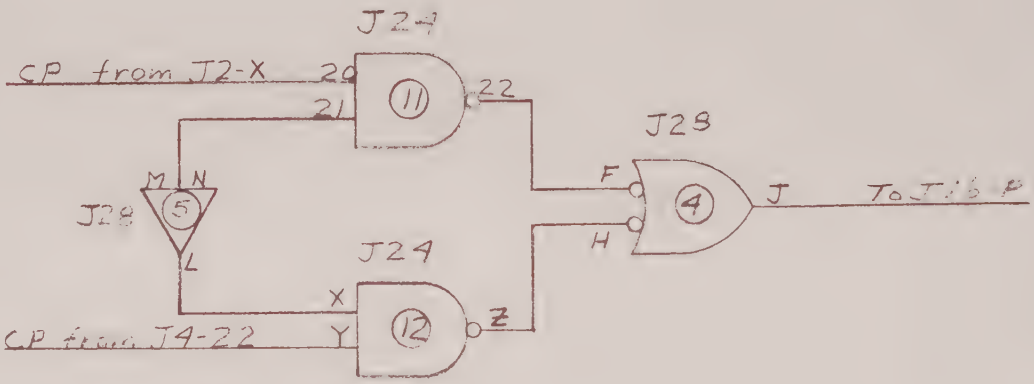
DATAPULSE
CULVER CITY
CALIFORNIA

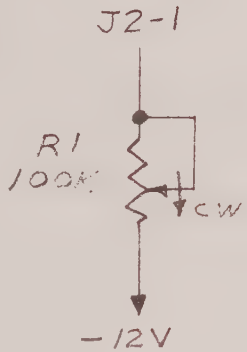
DWG A SIZE 40000-316

SCALE: CODE 15933 SHT 1 OF 1 REV A

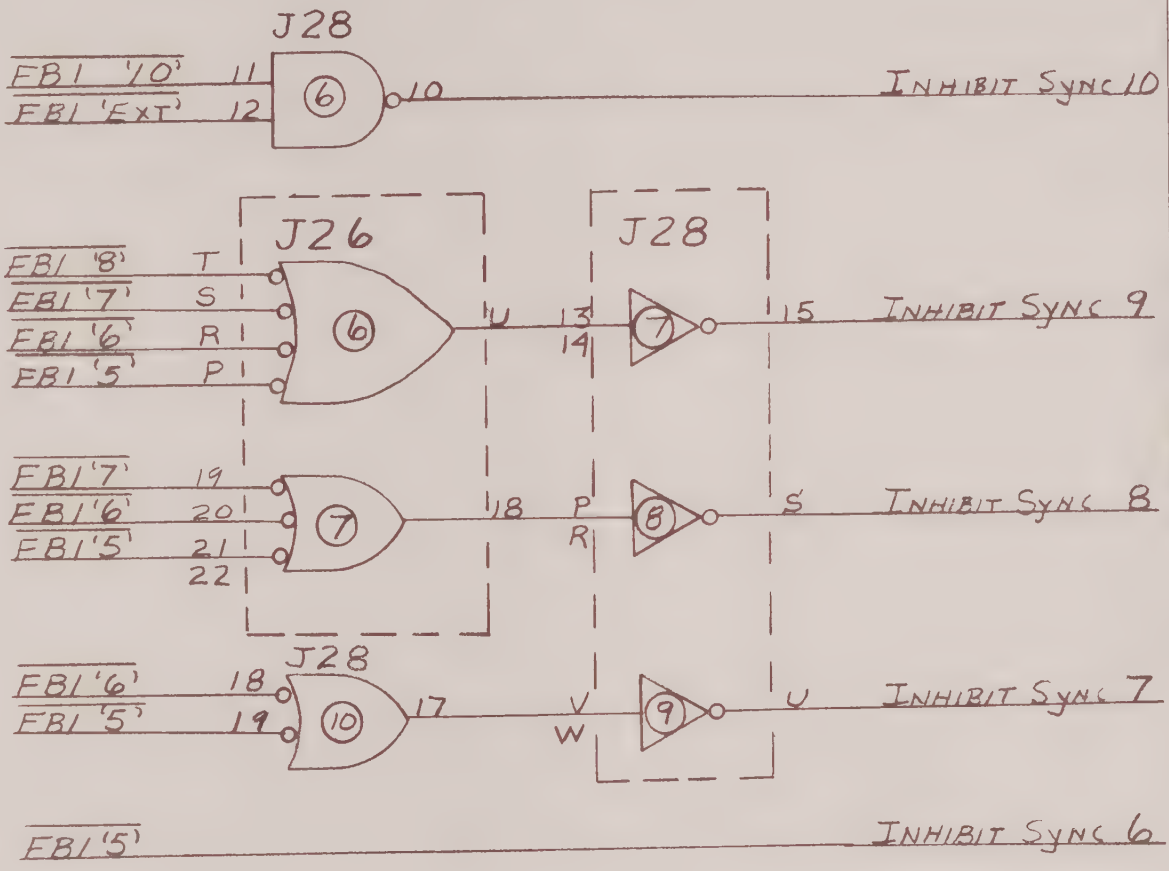
Clock Select

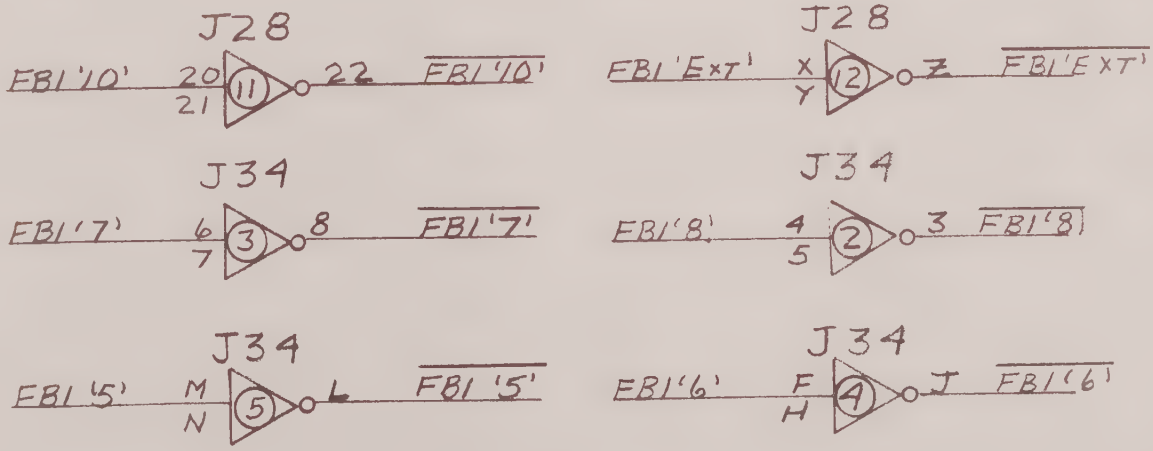






REVISIONS	APPROVALS		DATE	TITLE	
	DWN			SCHEMATIC DIAG.	DATAPULSE CULVER CITY CALIFORNIA
	CKD			CLOCK CONTROL	DWG A SIZE 40000-317
	APPD			MODEL 213A	
REV NO	REL			SCALE: CODE 15933	SHT 1 OF 1 REV A





DATAPULSE
CULVER CITY
CALIFORNIA

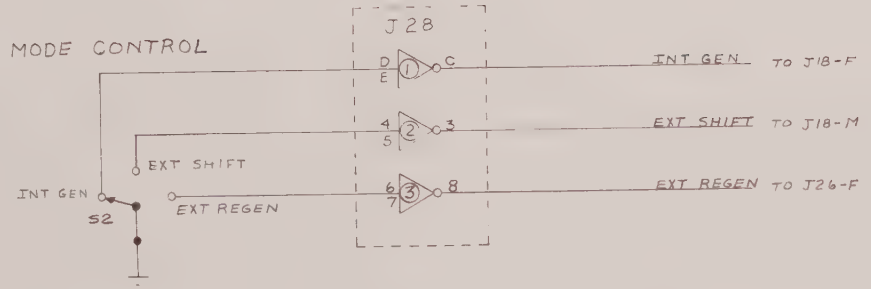
DWG A SIZE 40000-318 REV A
SHT 1 OF 1

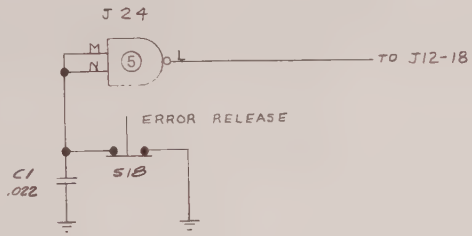
TITLE: SCHEMATIC DIAG. SYNC LENGTH CONT MODEL 213A
CODE 15933
SCALE:

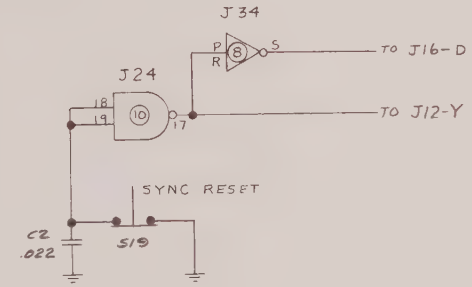
APPROVALS	DATE
DWN	5/96
CKD	5/96
APPD	5/96
REL	

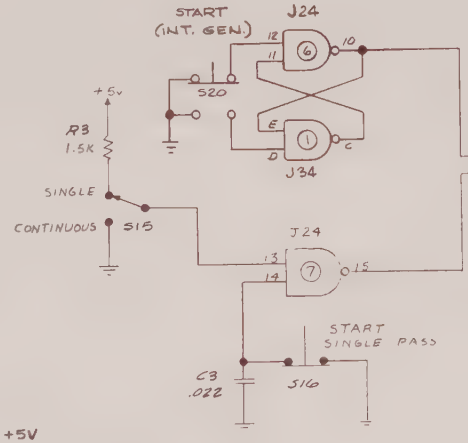
REVISIONS	REV NO.

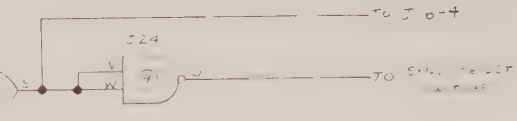
REVISIONS				
ECN	SYM	DESCRIPTION	DATE	APPROVAL

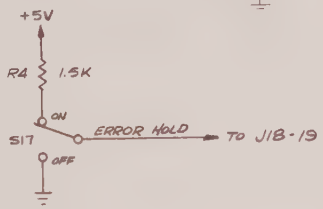












NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES			
TOLERANCES ON			
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	
MATERIAL			
FINISH			
DO NOT SCALE DWG.			

DRAWN		
CHECKED		
APPROVED		
APPROVED		
APPROVED		
RELEASED		

TITLE

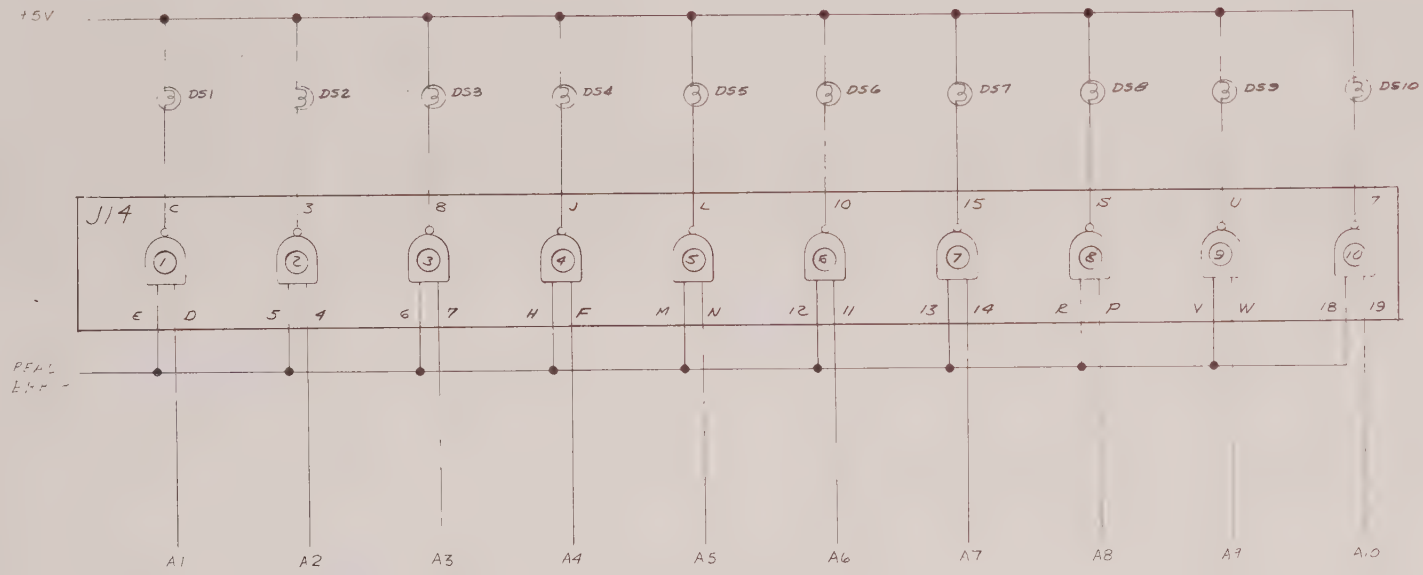
SCHEMATIC DIAGRAM MODE CONTROL MODEL 213A

DATAPULSE

DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG	
C SIZE	40000-323
SCALE	
SHEET	1 OF 1

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



Use [illegible] Dual-in-line
DTL
SOTH

UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES			
TOLERANCES ON			
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	
MATERIAL			
FINISH			
DO NOT SCALE DWG.			

DRAWN	[illegible]	3/10/1
CHECKED	[illegible]	3/10/1
APPROVED	[illegible]	3/10/1
APPROVED		
APPROVED		
RELEASED		

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

TITLE

SCHEMATIC DIAGRAM
ERROR PATTERN
READOUT
MODEL 2134

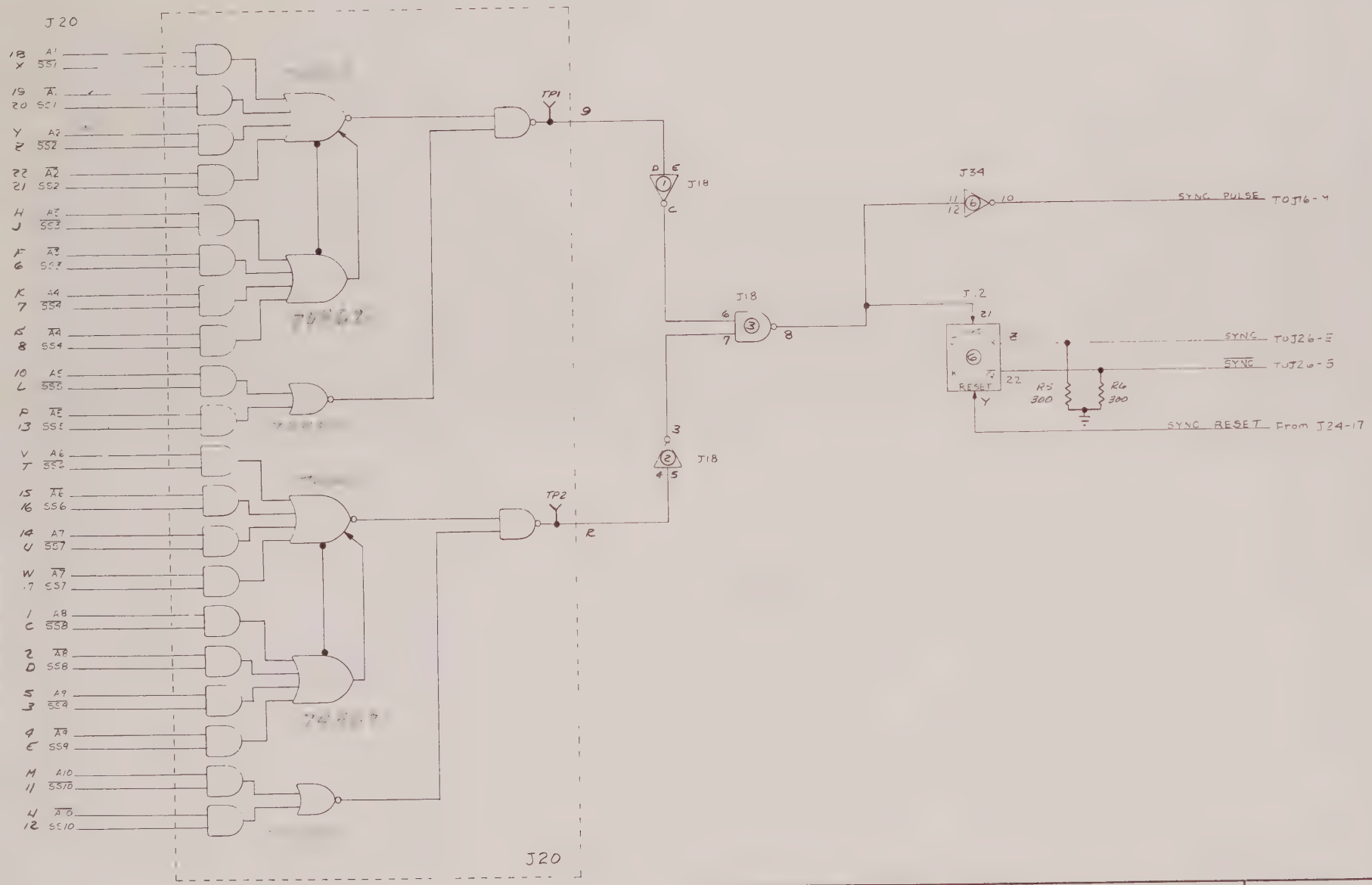
SCALE

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG	
SIZE C	40000-324
SHEET 1	OF 1

74H00N
SN74H62N
74H50
SN74H53N

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



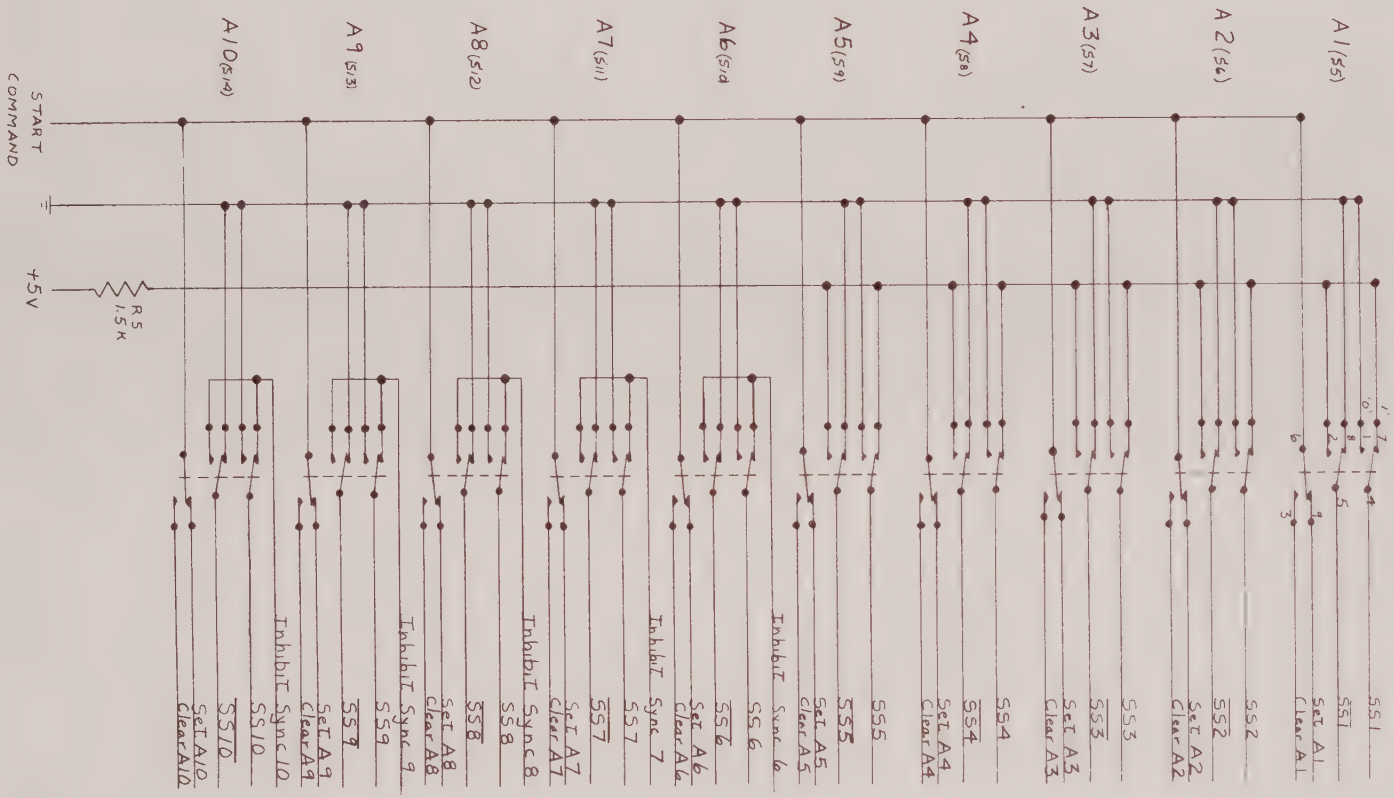
UNLESS OTHERWISE SPECIFIED			DRAWN		TITLE
DIMENSIONS ARE IN INCHES			CHECKED		SCHEMATIC DIAGRAM
TOLERANCES ON 3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	APPROVED		SYNC PATTERN GENERATION
MATERIAL			APPROVED		MODEL 213A
FINISH			APPROVED		
DO NOT SCALE DWG.			RELEASED		

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG	
SIZE	C
	40000-325
SCALE	
SHEET	1 OF 1

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



A

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED			DRAWN	8/2/63
DIMENSIONS ARE IN INCHES			CHECKED	8/3/63
TOLERANCES ON			APPROVED	8/6/63
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	APPROVED	
MATERIAL			APPROVED	
FINISH			RELEASED	

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DO NOT SCALE DWG.

TITLE
SCHEMATIC DIAGRAM
SYNC PATTERN
SELECT
MODEL 213A

SCALE | CODE 15933

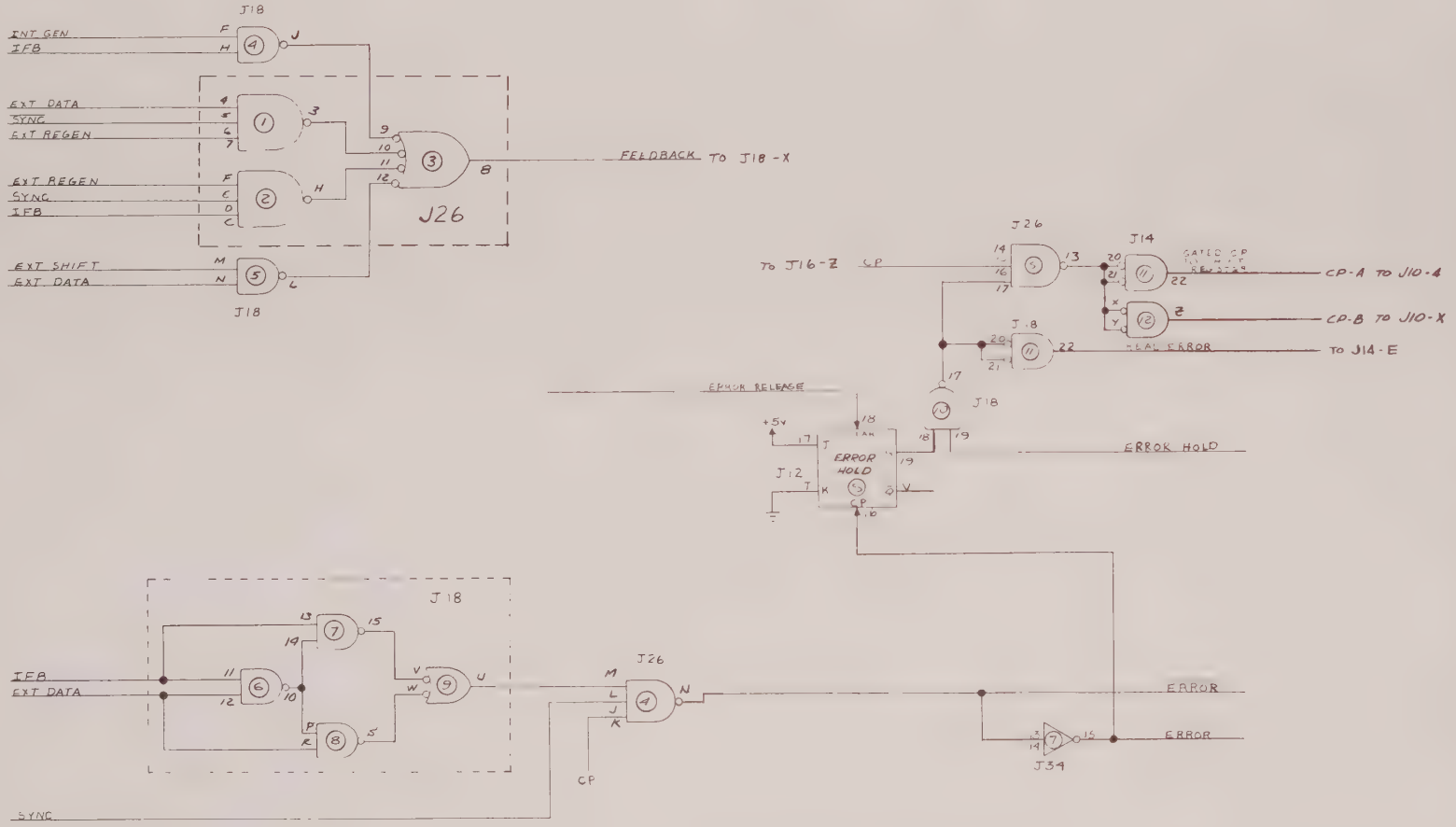
DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG C SIZE 40000-326

SHEET 1 OF 1

K+E ALBANENE® LA 2722

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL
/	A	Remove Single Pass Interrupt		
/	B	REVISED & REDRAWN	10JAN69	[illegible]



40000-327 B

UNLESS OTHERWISE SPECIFIED			DRAWN		
DIMENSIONS ARE IN INCHES			CHECKED		
TOLERANCES ON			APPROVED		
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	APPROVED		
MATERIAL			APPROVED		
FINISH			RELEASED		

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DO NOT SCALE DWG.

TITLE: SCHEMATIC DIAGRAM ERROR HOLD & FEEDBACK CONTROL MODEL 213A

DATAPULSE, INC.
CULVER CITY, CALIFORNIA

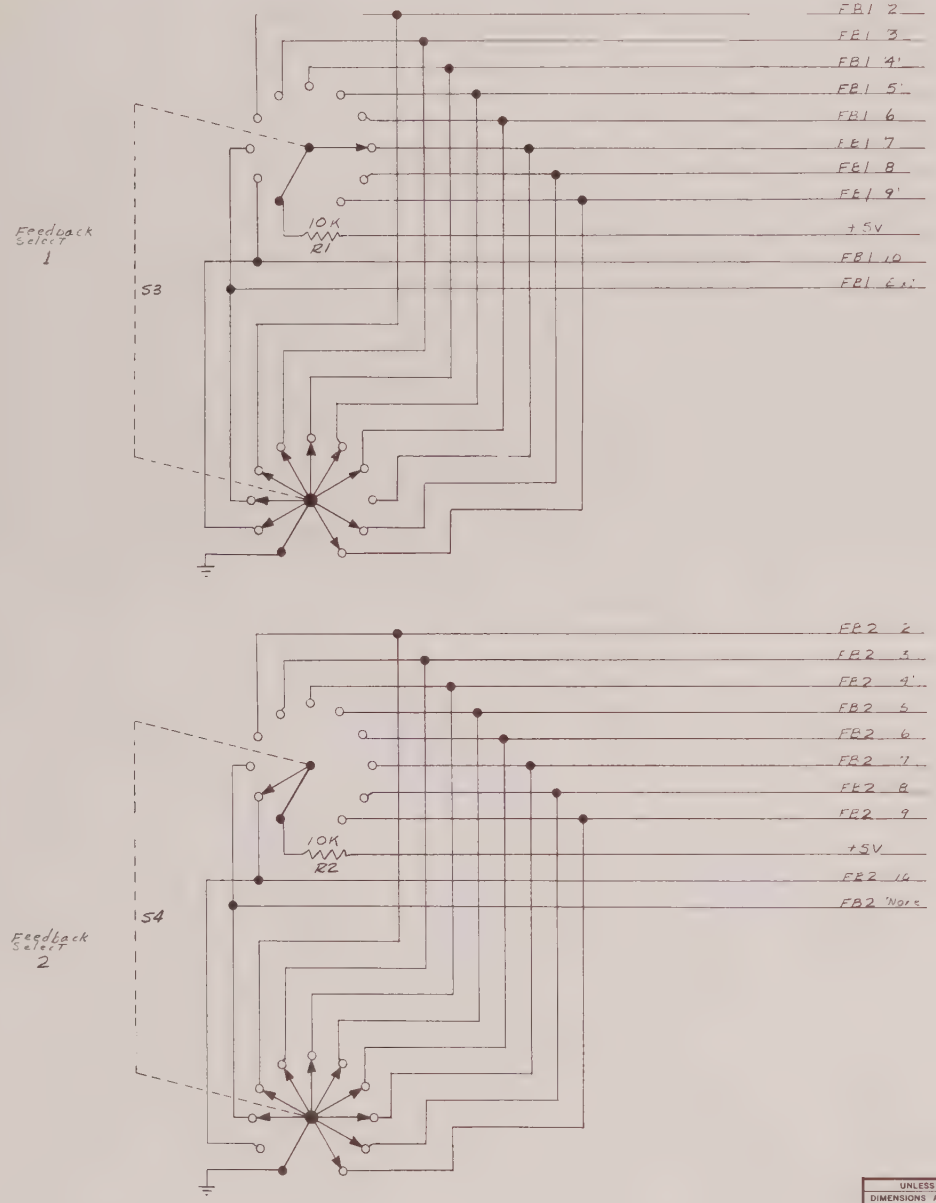
DWG C SIZE 40000-327

SCALE

SHEET / OF /

K+E ALBANENE® LA 2338

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL



NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED		
DIMENSIONS ARE IN INCHES		
TOLERANCES ON		
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±
MATERIAL		
FINISH		
DO NOT SCALE DWG.		

DRAWN		5/3/64
CHECKED		5/3/64
APPROVED		5/3/64
APPROVED		
APPROVED		
RELEASED		

TITLE

SCHEMATIC DIAGRAM
FEEDBACK SELECTION

MODEL 213A

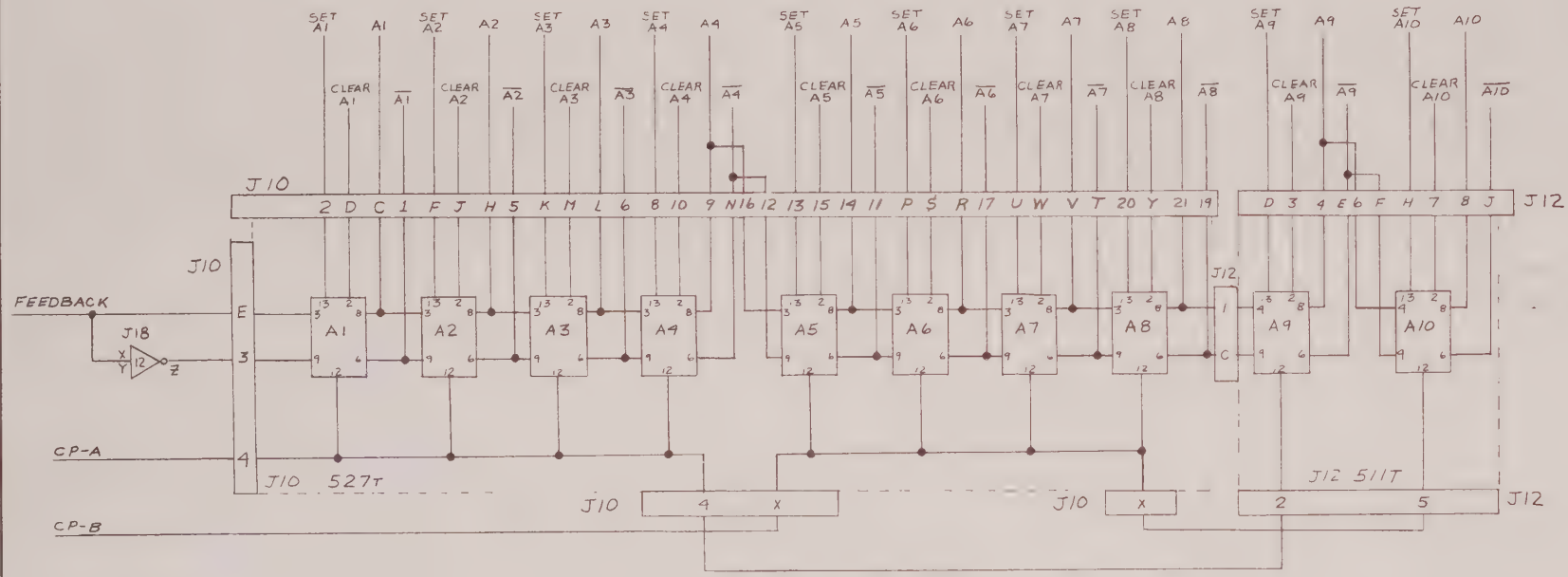
SCALE

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG
C
SIZE
40000-329

SHEET , OF /

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL
		Removed Loading Resistors		



NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES			
TOLERANCES ON			
3 PLACE DEC. ±	2 PLACE DEC. ±	ANGLES ±	
MATERIAL			
FINISH			
DO NOT SCALE DWG.			

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DRAWN		8/1/68
CHECKED		8/9/68
APPROVED		8/9/68
APPROVED		
APPROVED		
RELEASED		

TITLE: SCHEMATIC DIAGRAM SHIFT REGISTER Model 213A

SCALE | CODE 15933

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG C SIZE 400W-330

SHEET 1 OF 1

K&E ALBANENE® LA 2722

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL
/	A	REVISED & REDRAWN	11/10/69	LL HMN

CLOCK J40 → J4-3

DATA J41 → J6-3

FEED-BACK J42 → J8-3

INPUTS

ERROR J43 → J32-15

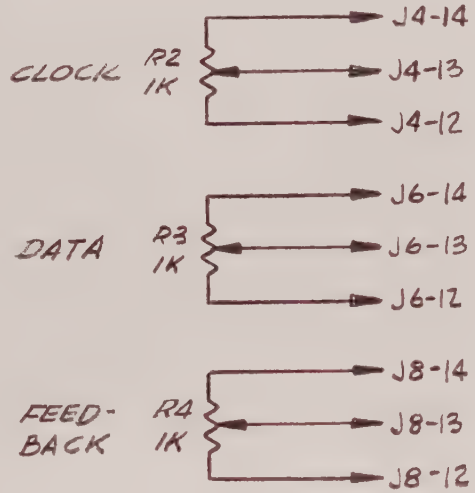
CLOCK J44 → J30-Z

SYNC J45 → J30-5

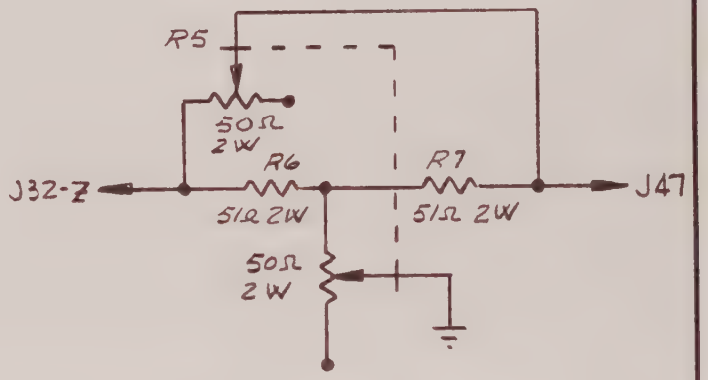
FEED-BACK J46 → J30-15

DATA J47 → TO BRIDGE T

OUTPUTS



THRESHOLD CONTROLS



DATA AMPLITUDE CONTROL

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED			DRAWN		
DIMENSIONS ARE IN INCHES				HWM	5/3/68
TOLERANCES ON			CHECKED		
3 PLACE DEC.	2 PLACE DEC.	ANGLES			
±	±	±	APPROVED		
MATERIAL			APPROVED		
FINISH			APPROVED		
DO NOT SCALE DWG.			RELEASED		

TITLE

SCHEMATIC DIAGRAM

INPUT / OUTPUT CONTROLS

MODEL 213A

SCALE

DATAPULSE

DATAPULSE, INC.

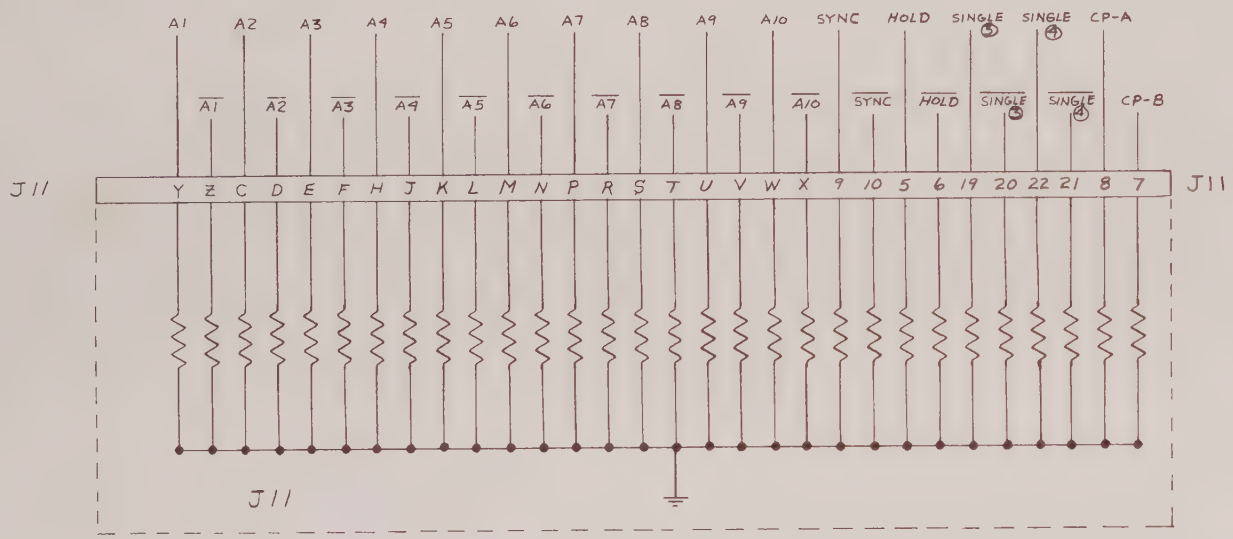
CULVER CITY, CALIFORNIA

DWG A SIZE

40000-331

SHEET 1 OF 1

REVISIONS				
E.C.N.	SYM	DESCRIPTION	DATE	APPROVAL


A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 SYNC HOLD SINGLE (5) SINGLE (4) CP-A
$\overline{A1}$ $\overline{A2}$ $\overline{A3}$ $\overline{A4}$ $\overline{A5}$ $\overline{A6}$ $\overline{A7}$ $\overline{A8}$ $\overline{A9}$ $\overline{A10}$ $\overline{SYNC}$ $\overline{HOLD}$ $\overline{SINGLE}$ (5) $\overline{SINGLE}$ (4) CP-B
J11
Y Z C D E F H J K L M N P R S T U V W X 9 10 5 6 19 20 22 21 8 7
J11
J11

NOTES: UNLESS OTHERWISE SPECIFIED
All Resistors 300 Ω

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
3 PLACE DEC. ± | 2 PLACE DEC. ± | ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DWG.

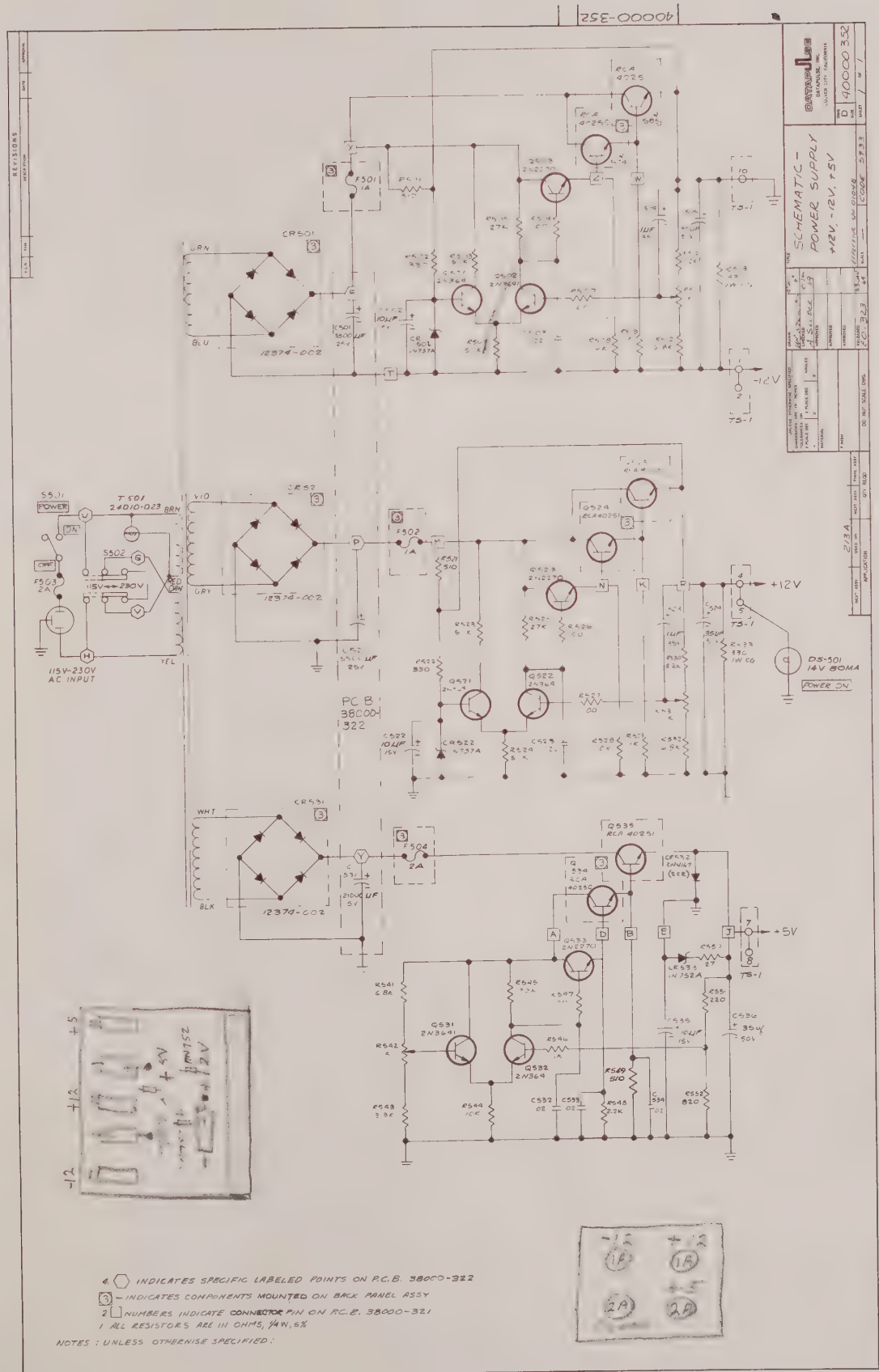
DRAWN		8/2/68
CHECKED		8/2/68
APPROVED		8/2/68
APPROVED		
APPROVED		
RELEASED		

TITLE
SCHEMATIC DIAGRAM
REGISTER LOADING
MODEL 213A

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

SCALE	CODE 15933	DWG SIZE C	40000-332
		SHEET / OF /	

K+E ALBANENE® LA 2722


SCHEMATIC - POWER SUPPLY +12V, -12V, +5V
DATAPULSE, INC.
SIZE 400CO 352
SHEET 1 OF 1
CODE 59333
REVISIONS
S501 POWER
T501 24010-023
F501 1A
F502 1A
F503 2A
S502
115V-230V
115V-230V AC INPUT
CR501
CR502
CR531
12374-002
PC B 38000-322
Q529 RCA 40251
Q530 RCA 40250
Q531 2N3691
Q532 2N3691
Q533 2N2270
Q535 RCA 40251
CR532 1N647 (SCR)
CR533 1N752A
+12V
-12V
+5V
TS-1
DS-501 14V 80MA
POWER ON
4. ⬡ INDICATES SPECIFIC LABELED POINTS ON P.C.B. 38000-322
3 □ - INDICATES COMPONENTS MOUNTED ON BACK PANEL ASSY
2 □ NUMBERS INDICATE CONNECTOR PIN ON P.C.B. 38000-321
1 ALL RESISTORS ARE IN OHMS, 1/4W, 5%
NOTES : UNLESS OTHERWISE SPECIFIED :

ADDENDA AND ERRATA

E. O. NO.	EFFECTIVE DATE	DWG. NO.	CHANGE
2518	7-25-68	Manual	Para. 1.3.2: Change from "30 MS" to "30 ns".
2532	8-1-68	Manual	Eliminate ALL references to "overshoot, undershoot, ringing, top slope, pulse aberrations, baseline aberrations and any other reference to pulse shape other than rise time, fall time, amplitude, duration, polarity and source or load impedance!'
8001	8-29-68	Manual	Change List of Schematics, Page iv as follows: Add: 41000-194 Logic Diagram Feedback Generation 40000-332 Schematic Diagram Register Loading Change letter "A" to the following: 40000-316, 317, 318, 326, 327, & 330. Delete: 40000-328 Schematic Diagram - Feedback Generation
2617	10-30-68	Manual	Para. 4.12.1 - Change R1, 100K, P/N 20053-104 TO 100K, P/N 20049-104.
2632	12-2-68	12154-030	In all applications, change diode - zener from 3.3V, .400mW, 10% (1N746) to 3.3V, .400mW, 5%(1N746A).
2635	12-10-68	40000-315	Schematic - Output Buffer 1. Add note 4 to general notes; "Factory adjust, may or may not be present", and add (*). 2. Add an asterisk (*) after CR1, CR2, and CR3.
2662	1-21-69	Manual	Section 4, Para. 4.3.4 - Transistor "TZ-82", P/N 12695-007 is an acceptable substitute of 2N3565, P/N 12695-003.

ADDENDA AND ERRATA

Model 213A

E. O. NO.	EFFECTIVE DATE	DWG. NO.	CHANGE
2715	4-30-69	40000-228	Change R7 from 2.5K to 2K, 1 W.
2717	5-5-69	40000-228	1. Change R1 from 220 ohm to 510 ohm. 2. Change +5 at R1 to +12. 3. Add C11, 33* across C8. 4. Add note 4: (*) asterisk indicates a factory selected value (may or may not be present).
2716	5-5-69	40000-315	Change R9 and 19 from 36 ohm, 2W to 33 ohm, 1 W, CG.
2729	6-5-69	40000-205	1. Connect pins 3, 4 & 5 together on A9 & A10 2. Connect pins 9, 10 & 11 together on A9 & A10
2730	6-5-69	40000-207	1. Connect pins 3, 4 & 5 together on all I.C.s. 2. Connect pins 9, 10, & 11 together on all I.C.s.
2752A (A change corrects Schematic	8-19-69 # 2-27-70)	40000-315	Schematic - Output Buffer R20, 820 ohm, 1/4W should be changed to 1/2W.
2662A	9-23-69	Manual	Optional Change: Transistor "TZ-82". P/N 12695-007 is an acceptable substitute for 2N3565, P/N 12695-003.
2716A	10-23-69	40000-315	Change R29 from 36 ohm, 2W to 27 ohm, 1W, CG.
2797	11-5-69	40000-315	Change R9 & 19 from 33 ohm, 1W, P/N10722-330 to 27 ohm, 1W, CG, P/N10722-270.
2893	2-13-70	40000-352	Schematic - Power Supply, +12V, -12V, +5V - Change C503, C523, C532, C533, C534 from .02, P/N 11123-223 to .022μF, 25V, P/N 11241-223.

MODEL 213A CHECKOUT PROCEDURE

1. Equipment (or equivalent) Required

   a. A Datapulse Model 101 Pulse Generator.

   b. A Datapulse Model 201 Data Generator.

   c. Five Tektronix Type 012-0057-01, 50 ohm coaxial cables (with BNC connectors).

   d. Five Tektronix Type 011-0049-00, 50 ohm terminations (with BNC connectors).

   e. A Tektronix Type 544 Oscilloscope with a Type 1A2 Dual-Trace Plug-in Unit.

2. POWER and ERROR PATTERN Lamps

   a. Set the instrument controls as follows:

Control	Setting
POWER switch	ON
CLOCK SELECT range switch	10 MHz
CLOCK SELECT vernier	fully clockwise
MODE SELECT switch	INT GEN
SYNC PATTERN SELECT switches	all to "1"
FB 1 switch	A10
FB 2 switch	None
ERROR HOLD switch	ON
DATA AMPLITUDE control	fully clockwise
SINGLE PASS switch	CONTINUOUS

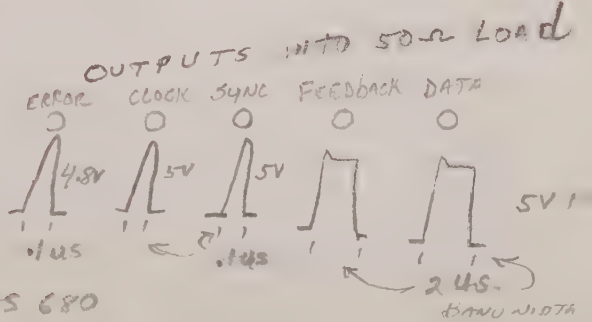
   b. Observe that the POWER lamp is lighted.

   c. Observe that when the START (INT GEN) pushbutton is actuated, all the ERROR PATTERN lamps are lighted.

3. Output Amplitudes

   a. Set the instrument controls as follows:

Control	Setting
SYNC PATTERN SELECT switches	A1, A3, A5, A7, A9 to "1" A2, A4, A6, A8, A10 to "0"
ERROR HOLD switch	OFF
Remaining controls	as before



5.5V 5.5V 5.5V 5.5V

b. Observe that ERROR, CLOCK, FEEDBACK, and SYNC output amplitudes are +5V, ±10% into 50 ohms.

c. Observe that DATA OUTPUT amplitude is variable from +0.6V to +5V into 50 ohms. OK

NOTE: Use internal scope sync.

4. CLOCK SELECT

a. Retain the previous settings.

b. Observe the DATA OUTPUT on the oscilloscope and check for proper pulse width range from 100 ns to 100 ms to assure clock rate ranges from 10 MHz to 10 Hz; be sure there is overlap of the CLOCK SELECT ranges. ✓

NOTE: If no outputs or erratic outputs initially are present, actuate the START (INT GEN) pushbutton.

c. Set the CLOCK SELECT range switch to EXT and feed in a ±1V to ±5V (terminated into 50 ohms) signal from 10 MHz to 10 Hz and with a minimum duration of 30 ns at the EXT CLOCK INPUT connection.

d. Using internal scope sync and properly setting the EXT CLOCK THRESHOLD level, observe an output at the DATA OUTPUT connection (see NOTE above).

5. EXT REGEN Mode

a. Set the instrument controls as follows:

Control	Setting
CLOCK SELECT range switch	10 MHz
CLOCK SELECT vernier	fully clockwise
MODE SELECT switch	EXT REGEN
FB 1 switch	A8
FB 2 switch	NONE
SYNC PATTERN SELECT switches	A3, A6, A7, A8 to "1" A1, A2, A4, A5 to "0" A9, A10 to either

b. On the Model 201, set the instrument controls as follows:

Control	Setting
BASELINE level	0 V
AMPLITUDE control	1V

Control	Setting
RECYCLE switch	AUTO
CLOCK SLOPE switch	(-)
DATA CONTENT switches	1, 2, 3, 6, 9, 10, 11, 14 to "1" 4, 5, 7, 8, 12, 13, 15, 16 to "0"

c. Connect the equipment (as shown in Figure 1), and adjust Model 201 TRIGGERING LEVEL for stable output.

d. Monitor the 213A ERROR and DATA outputs on the scope and actuate the SYNC RESET pushbutton of the 213A. The ERROR OUTPUT should reduce to 0 V with no pulses present. If pulses are present, check:

1. 201 DATA CONTENT switches.
2. 213A SYNC PATTERN SELECT switches.
3. 201 TRIGGERING LEVEL
4. 213A EXT DATA THRESHOLD level.

NOTE: The pattern set into the 213A SYNC PATTERN SELECT switches A1-A8 must be the reverse of the pattern set into the 201. With the FB 1 control set to A8 as stated above, SYNC PATTERN SELECT switches A9 and A10 do not affect the pattern.

e. After the 201 and 213A have been properly synchronized and no errors are present, change any DATA CONTENT switch of the 201 and an error pulse should appear at the 213A ERROR OUTPUT. If two data switches are changed, two error pulses should appear, etc. With the DATA CONTENT switches returned to their original condition, all error pulses should be removed.

6. ERROR HOLD

a. Retain the connections of Figure 1 and set the instrument controls as follows:

Control	Setting
FB 1 switch	A8
FB 2 switch	NONE
SYNC PATTERN SELECT switches	A3, A6, A7, A8 to "1" A1, A2, A4, A5 to "0" A9, A10 to either
ERROR HOLD switch	ON

b. Actuate the SYNC RESET pushbutton, then the RELEASE pushbutton. The 213A should operate with no ERROR OUTPUT.

c. Change any DATA CONTENT switch setting on the 201. Observe that the 213A stops generating data and the ERROR PATTERN lamps are lighted. ERROR PATTERN lamp A1 will show what error bit was changed from; lamps A2 through A9 will indicate the previous nine bits of data.

d. To restart the 213A, return the 201 DATA CONTENT switches to their original condition. Actuate the SYNC RESET pushbutton, then the RELEASE pushbutton. The 213A is now ready to look for the next error in the incoming data at which it will stop as before.

7. SINGLE PASS

a. Disconnect the 201 and set the 213A instrument controls as follows:

Control	Setting
FB 1 switch	A10
FB 2 switch	A3 or A7
CLOCK SELECT range switch	.1 KHz
CLOCK SELECT vernier	fully clockwise
MODE SELECT switch	INT GEN
SINGLE PASS switch	SINGLE

b. Observe that a single DATA OUTPUT sequence of approximately three seconds is obtained by actuating either START pushbutton.

8. Feedback

The EXT FEEDBACK THRESHOLD level, the EXT FEEDBACK INPUT connection, and the FB 1 EXT setting are used only when cascading two or more 213A's.

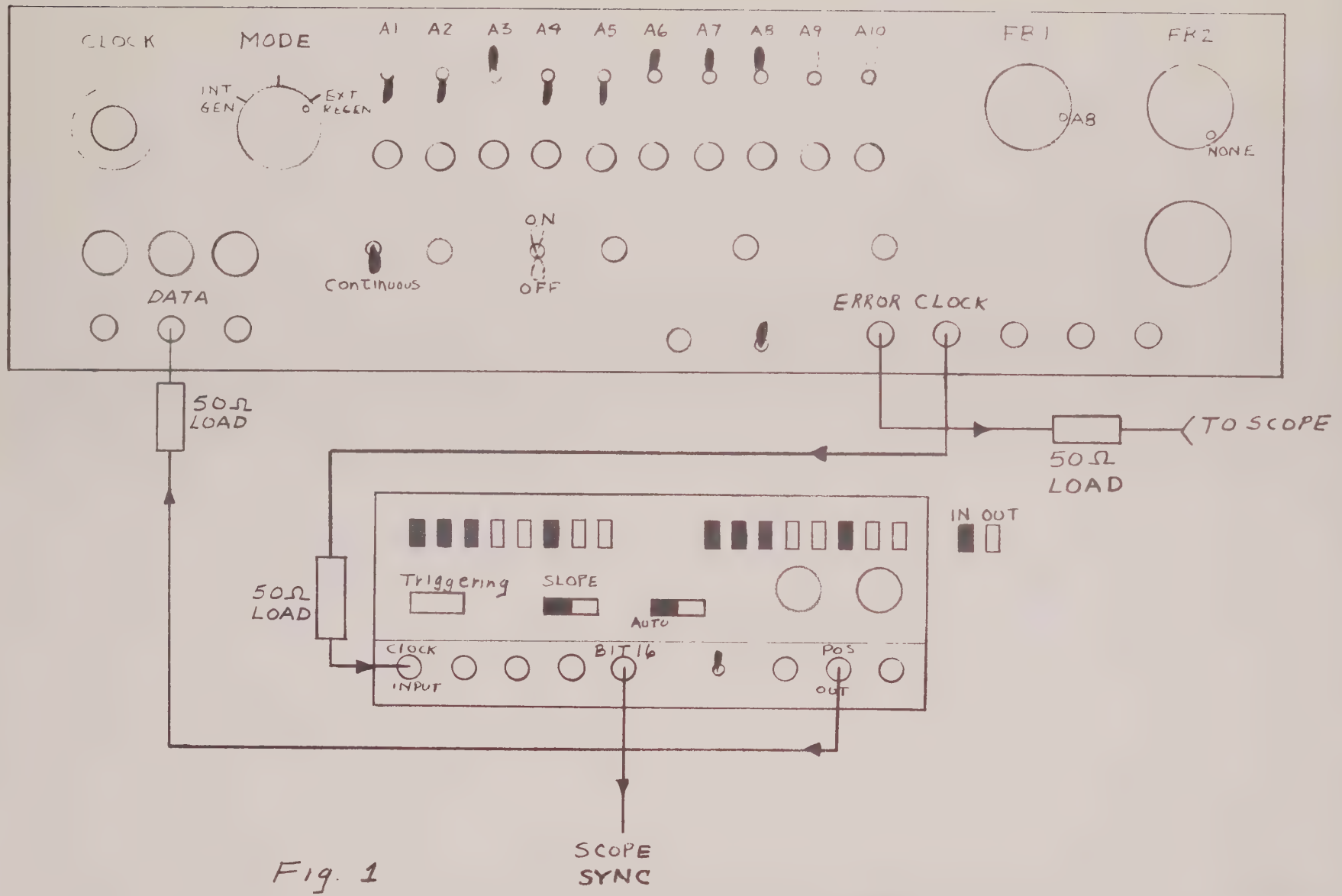


Fig. 1

REVISIONS	REV NO.	APPROVALS	DATE
	DWN		
	CKD		
	APPD		
	REL		

TITLE

DATAPULSE
CULVER CITY
CALIFORNIA

DWG A SIZE

SCALE: | CODE 15933 | SHT OF | REV

SEMICONDUCTOR REPLACEMENTS

(Applicable to all Datapulse Models except the Model 102).

FROM DATAPULSE DIVISION

SERVICE BULLETIN NO. 1-65
Revised 2-19-70

The listed commercial equivalent diodes and transistors are suitable replacements for the corresponding Datapulse parts, either as direct substitutes, or as selected for the special performance characteristics given.

DATAPULSE TYPE NO.	DATAPULSE PART NO.	COMMERCIAL EQUIVALENT
Diodes:		
DP15-0	22154-000	1N752A selected for $\Delta V < 0.2V$ between 7mA and 110mA.
DP15-1	22154-001	Same as DP15-0 but matched in pairs to within 0.1V.
DP15-201	22154-201	1N936 selected for 9.4V±0.1V @25mA.
DP16-0	22164-000	1N3600
DP16-1	22164-001	1N3604
DP16-2	22164-002	HPA1003
DP19-0	22194-000	1N2070/1N4005
DP19-1	22194-001	1N4002
DP19-6	22194-006	1N2071/1N4005
Transistors:		
DP43-0	22435-000	2N984
DP46-0	22465-000	2N2964A
DP46-1	22465-001	Selected for h_{fe} = 100 min.
DP59-0	22595-000	2N2904A
DP60-0	22605-000	2N2411
DP60-1	22605-001	2N2894 selected for V_{ceo} (sust) = 20V min.
DP60-2	22605-002	2N2904 or 2N3133
DP60-3	22605-003	2N2894
DP60-4	22605-004	2N3209
DP60-5	22605-005	FT1702
DP60-6	22605-006	2N3640
DP60-7	22605-007	2N2894 selected for V_{ceo} (sust) = 25V.
DP63-0	22635-000	2N2369 or 2N2501
DP63-1	22635-001	2N3723
DP63-2	22635-002	Replaced by DP63-3
DP63-3	22635-003	2N2369A (Fairchild)
DP63-4	22635-004	2N3646 or 2N2369A
DP63-6	22635-006	2N2270
DP63-7	22635-007	2N3261 selected for C_{OB} of 3.3pF or less
DP63-8	22635-008	May be replaced by 2N5109 selected for $h_{fe} \geq 20$ @I_c = 0.25A & V_c = 2.5V
DP63-9	22635-009	May be replaced by 2N5109 selected for $h_{fe} \geq 20$ @I_c = 0.25A & V_c = 2.5V
DP64-0	22645-000	May be replaced by 2N5109 selected for $h_{fe} \geq 20$ @I_c = 0.25A & V_c = 2.5V

DATAPULSE DIVISION
SYSTRON DONNER CORPORATION

10150 W. Jefferson Blvd., Culver City, California 90230
Phone: (213) 836-6100 • TWX: 910-340-6766

In Europe: Systron-Donner International, S.A., 447, Ave. De Tervueren, Brussels 15, Belgium
Phone: 71-76-84 • Telex: 23606 Belgium

WARRANTY

Datapulse Incorporated warrants each instrument of its manufacture to be free from defects in material and workmanship. Our obligation under this Warranty is limited to servicing or adjusting any instrument returned to our factory for that purpose, and to making good at our factory any part or parts thereof except tubes, transistors, fuses or batteries which shall, within one year after making delivery to the original purchaser, be returned to us with transportation charges prepaid, and which our examination shall disclose to our satisfaction to have been thus defective.

Instruments returned under this Warranty will not be accepted at the Datapulse plant without prior authorization by a Datapulse representative or by the service manager of Datapulse Incorporated.

Datapulse Incorporated reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This Warranty is expressly in lieu of all other obligations or liabilities on the part of Datapulse Incorporated and Datapulse Incorporated neither assumes nor authorizes any other person to assume for them any other liability in connection with the sales of Datapulse Incorporated instruments.

www.manualsplus.com
1011353